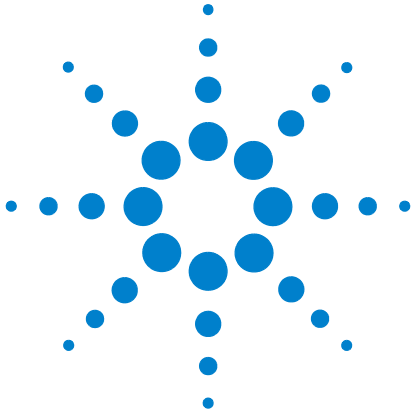

Agilent N5413A DDR2 Compliance Test Application

Compliance Testing Notes

Agilent Technologies

Notices

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DDR2 —An Overview

DDR2 is the current state of the art in the industry standard DRAM and the driver for the next several years in all types of memory design. DDR2-SDRAM is an evolutionary upgrade over the existing DDR memory. It maintains the same core functions of DDR: transferring 64 bits of data twice every clock cycle, twice that of the front-side bus (FSB) of a computer system (for effective transfer rate). DDR2-SDRAM also introduces features and functions that go beyond the DDR-SDRAM specifications, enabling DDR2 to operate at the data rates of 400 MHz, 533 MHz, 677 MHz and 800 MHz.

Table 1 General Characteristics and Specifications of DDR2

Component Speed	Module Speed	Front Side Bus Speed	Data Rate	Module Bandwidth	Dual-Channel System Bandwidth
DDR2-400	PC2-3200	200 MHz	400 MT/s	3.2 GB/sec	6.4 GB/sec
DDR2-533	PC2-4300	266 MHz	533 MT/s	4.3 GB/sec	8.6 GB/sec
DDR2-667	PC2-5300	333 MHz	667 MT/s	5.3 GB/sec	10.6 GB/sec
DDR2-800	PC2-6400	400 MHz	800 MT/s	6.4 GB/sec	12.8 GB/sec

Changes in the DRAM architecture and signaling as well as additions to the mode register, have resulted in the significant advancement of DDR2. The changes in DRAM architecture have double the bandwidth without increasing the demand on the DRAM core, while keeping the power low. Modifications to the DRAM architecture include:

- Shortened row length for reduced activation power.
- Burst length of four and eight for improved data bandwidth capability.
- Addition of eight banks for 1 Gb densities and above.

The DDR architecture is source synchronous. The data is captured twice per clock cycle using the bi-directional data strobe signal. This architecture uses a 4n prefetch architecture, where the internal data bus is four times the size of the external data bus. The signal interface is SSTL_18. Stub Series Terminated Line for 1.8 Volts (SSTL_18) is a standard approved by JEDEC.

Another new feature in DDR2 is, it uses FBGA (Fine Ball Grid Array) packaging to reduce inductance. This method allows higher memory densities with better electrical and thermal properties in considerably smaller chips.

Table 2 Features and Advantages of DDR2

Feature/Option	DDR2
Package	FBGA only
Voltage	1.8 V, 1.8 V I/O
Densities	256 Mb - 2 Gb
Internal Banks	4 and 8
Prefetch (MIN WRITE Burst)	4
Speed (Data Pin)	400 MHz, 533 MHz 667 MHz and 800 MHz
Termination	DRAM on-die termination (ODT), optional on motherboard termination
Data Strobes	Differential or single-ended
Modules	240-pin DIMM unbuffered registered 200-pin SODIMM 244-pin MicroDIMM

DDR2 is not backward compatible with DDR. Even though DDR2 modules and DDR modules have the same length, they have differences in the connectors, signaling and supply voltages. Thus, DDR2 modules cannot be used in the DDR system.

For both DDR and DDR2, the signal integrity is measured at the balls of the DRAM, where the JEDEC Specification is defined upon.

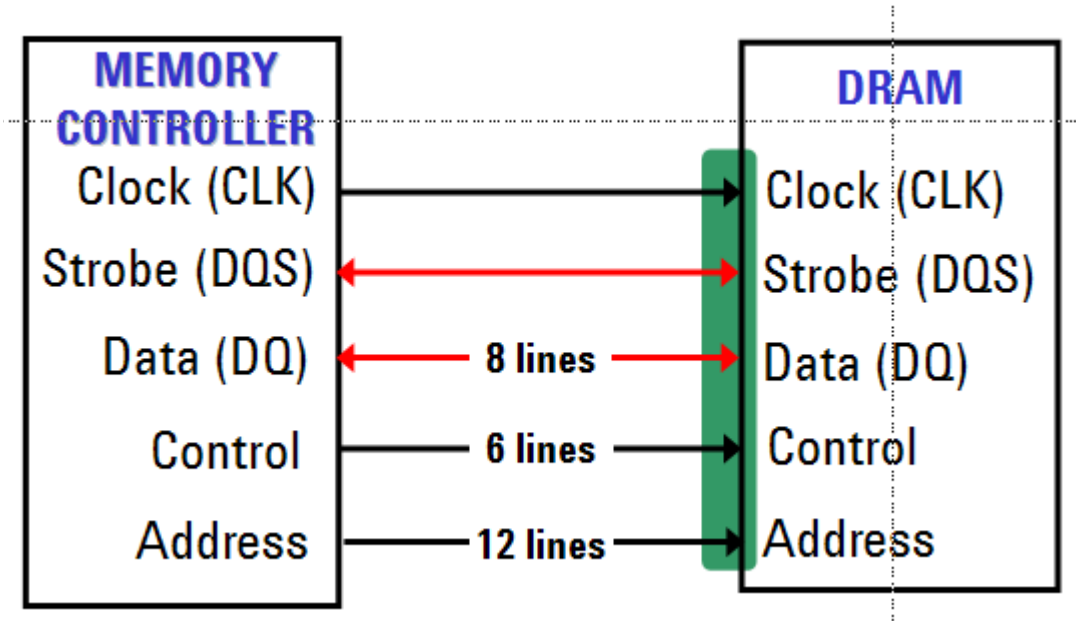

Figure 1 DDR Signal Integrity

To obtain the best result, you may follow either one of the below probing method:

- Probing at via holes - since you are measuring the signals closest to the balls of the DRAM.
- Probing on the DIMM side of the 22Ω resistors.

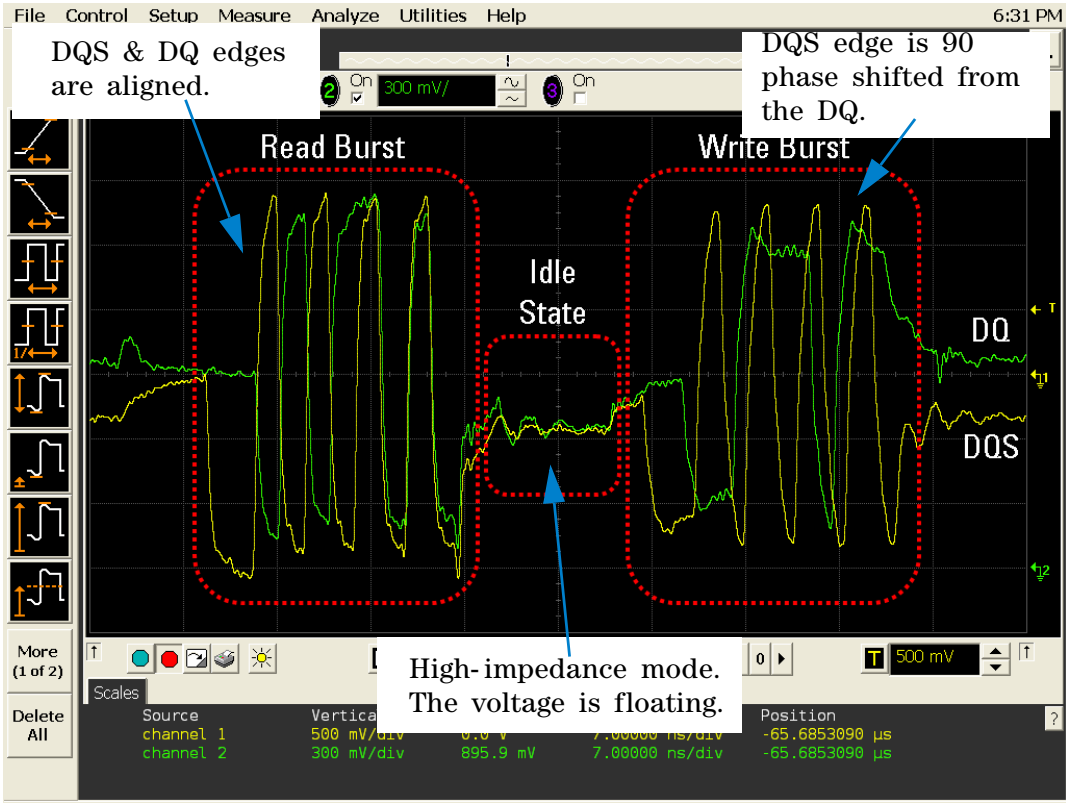

Figure 2 DDR Signal Characteristics

Figure 2 shows the DDR2 signals driven from the DRAM. It shows the Read burst, Write burst and the Idle State.

DDR2 —Quick Reference

Table 3 DDR2 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
tJIT(per)					√						√[2]				
tJIT(cc)					√						√[2]				
tERR(nper)					√						√[2]				
tCH(avg)					√						√[2]				
tCL(avg)					√						√[2]				
tJIT(duty)					√						√[2]				
tCK(avg)					√						√[2]				
VSWING (MAX)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
SlewR		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
SlewF		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIH(ac)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIH(dc)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIL(ac)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VIL(dc)		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
AC Overshoot		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
AC Undershoot		√	√	√	√	√	√	√	√[2]	√[2]	√[2]	√[2]	√[2]	√[2]	
VID(ac)		√		√	√					√[3]	√[3]				
VIX(ac)		√		√	√					√[3]	√[3]				
VOX(ac)		√		√						√[3]					
Eye Diagram - Read	√		√	√					√[2]	√[2]					
Eye Diagram - Write		√	√	√					√[2]	√[2]					

Table 3 DDR2 Cycles and Signals

NOTE: 1 = Single Ended probing; 2 = Differential probing; 3 = 2 x Single Ended probing

TEST	Cycle		Based on Test Definition						Required to Perform on Scope						Opt.
	Read	Write	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	DQ	DQS	CK	ADD	Ctrl	Data Mask Ctrl	CS#
High State Ringing			√	√		√	√	√	√[1,2]	√[1,2]		√[1,2]	√[1,2]	√[1,2]	
Low State Ringing			√	√		√	√	√	√[1,2]	√[1,2]		√[1,2]	√[1,2]	√[1,2]	
tAC	√		√		√				√[2]	√[2]	√[2]				√
tDQSCK	√			√	√				√[2]	√[2]	√[2]				√
tHZ(DQ)	√		√		√				√[2]	√[2]	√[2]				√
tLZ(DQS)	√			√	√				√[2]	√[2]	√[2]				√
tLZ(DQ)	√		√		√				√[2]	√[2]	√[2]				√
tDQSQ	√		√	√					√[2]	√[2]	√[2]				√
tQH	√		√	√					√[2]	√[2]	√[2]				√
tDQSS		√		√	√				√[2]	√[2]	√[2]				√
tDQSH	√			√					√[2]	√[2]	√[2]				√
tDQSL	√			√					√[2]	√[2]	√[2]				√
tDSS		√		√	√				√[2]	√[2]	√[2]				√
tDSH		√		√	√				√[2]	√[2]	√[2]				√
tWPST		√		√					√[2]	√[2]	√[2]				√
tWPRE		√		√					√[2]	√[2]	√[2]				√
tRPRE	√			√					√[2]	√[2]	√[2]				√
tRPST	√			√					√[2]	√[2]	√[2]				√
tDS(base)		√	√						√[2]	√[2]	√[2]				√
tDH(base)		√	√						√[2]	√[2]	√[2]				√
tDS1(base)		√	√		√				√[1]	√[1]	√[1]				√
tDH1(base)		√	√		√				√[1]	√[1]	√[1]				√
tIS(base)	√				√	√	√				√[2]	√[2]	√[2]		√
tIH(base)	√				√	√	√				√[2]	√[2]	√[2]		√

DDR2 Compliance Test Application — At A Glance

The Agilent N5413A DDR2 Compliance Test Application is a DDR2 (Double Data Rate 2) test solution that covers electrical, clock and timing parameters of the JEDEC (Joint Electronic Device Engineering Council) specifications, specifically *JESD79-2C* and *Intel DDR2 667/800 JEDEC Specification Addendum Rev 1.1*. The software helps you in testing all the un-buffered DDR2 device under test (DUT) compliance, with the Agilent 54850A, 80000 or 90000A Series Infiniium digital storage oscilloscope.

There are 2 main categories of test modes:

- Compliance Tests - These tests are based on the DDR2 JEDEC compliance specifications and are compared to corresponding compliance test limits.
- Advance Debug Tests - These tests are not based on any compliance specification. The primary use of these tests is to perform signal debugging.

The DDR2 Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Allows you to determine the number of trials for each test, with the new multi trial run capability.
- Provides detailed information of each test that has been run. The result of maximum twenty five worst trials can be displayed at any one time.
- Creates a printable HTML report of the tests that have been run.

The minimum number of probes required for the tests are:

- Clock tests - 1 probe.
- Electrical tests - 3 probes.
- Clock Timing tests - 3 probes.
- Advanced Debug tests - 3 probes.

NOTE The tests performed by the DDR2 Compliance Test Application are intended to provide a quick check of the physical layer performance of the DUT. These testing are not replacement for an exhaustive test validation plan.

DDR2 SDRAM electrical, clock and timing test standards and specifications are described in the *JESD79-2C* document. DDR2 SDRAM clock test standards and specifications are described in the *Intel DDR2 667/800*

JEDEC Specifications Addendum Rev 1.1 document. For more information, please refer to JEDEC web site at www.jedec.org.

Required Equipment and Software

In order to run the DDR2 automated tests, you need the following equipment and software:

- 54850A series, 80000 or 90000A Series Infiniium Digital Storage Oscilloscope. Agilent recommends using 4 GHz and higher bandwidth oscilloscope.
- Infiniium software revision A.05.20 or later.
- N5413A DDR2 Compliance Test Application, version 2.1 and higher.
- RAM reliability test software.
- 1169A, 1168A, 1134A, 1132A or 1131A InfiniiMax probe amplifiers.
- N5381A or E2677A differential solder-in probe head, N5382A or E2675A differential browser probe head, N5425A ZIF probe head or N5426A ZIF tips.
- Any computer motherboard system that supports DDR2 memory.
- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).

Below are the required licenses:

- N5413A DDR2 Compliance Test Application license.
- N5414A InfiniiScan software license.
- E2688A Serial Data Analysis and Clock Recovery software license.
- N5404A Deep memory option (optional).

In This Book

This manual describes the tests that are performed by the DDR2 Compliance Test Application in more detail; it contains information from (and refers to) the *JESD79- 2C* and *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*, and it describes how the tests are performed.

- Chapter 1, "Installing the DDR2 Compliance Test Application" shows how to install and license the automated test application software (if it was purchased separately).
- Chapter 2, "Preparing to Take Measurements" shows how to start the DDR2 Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, "Measurement Clock Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average high and low pulse width, half period jitter and average clock period tests.
- Chapter 4, "Single-Ended Signals AC Input Parameters Tests" shows how to run the single-ended signals AC input parameters tests. This chapter includes input signal maximum peak to peak swing tests, input signal minimum slew rate (rising) tests, input signal minimum slew rate (falling) tests, input logic high tests and input logic low tests.
- Chapter 5, "Single-Ended Signals Overshoot/Undershoot Tests" describes the AC overshoot and undershoot tests probing and method of implementation.
- Chapter 6, "Differential Signals AC Input Parameters Tests" describes the V_{ID} AC differential input voltage tests and V_{IX} AC differential cross point voltage tests.
- Chapter 7, "Differential Signal AC Output Parameters Tests" contains more information on the V_{OX} AC differential cross point voltage tests.
- Chapter 8, "Clock Timing (CT) Tests" describes the clock timing operating conditions of DDR2 SDRAM as defined in the specification.
- Chapter 9, "Data Strobe Timing (DST) Tests" describes various data strobe timing tests including tHZ(DQ), tLZ(DQS), tLZ(DQ), tDQSQ, tQH, tDQSS, tDQSH, tDQSL, tDSS, tDSH, tWPST, tWPRE, tRPRE and tRPST tests.
- Chapter 10, "Data Mask Timing (DMT) Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average high and low pulse width, half period jitter and average clock period tests.
- Chapter 11, "Command and Address Timing (CAT) Tests" describes the measurement clock tests including clock period jitter, clock to clock period jitter, cumulative error, average high and low pulse width, half period jitter and average clock period tests.

- Chapter 12, “Advanced Debug Mode Read-Write Eye-Diagram Tests” describes the user defined real-time eye-diagram test for read cycle and write cycle.
- Chapter 13, “Advance Debug Mode High-Low State Ringing Tests” shows the high state and low state ringing test method of implementation.
- Chapter 14, “Calibrating the Infiniium Oscilloscope and Probe” describes how to calibrate the oscilloscope in preparation for running the DDR2 automated tests.
- Chapter 15, “InfiniiMax Probing” describes the probe amplifier and probe head recommendations for DDR2 testing.
- Chapter 16, “Common Error Messages” describes the error dialog boxes that can appear and how to remedy the problem.

See Also

- The DDR2 Compliance Test Application’s online help, which describes:
  - Starting the DDR2 compliance test application.
  - Creating or opening a test project.
  - Setting up DDR2 test environment.
  - Selecting tests.
  - Configuring selected tests.
  - Connecting the oscilloscope to the DUT.
  - Running tests.
  - Viewing test results.
  - Viewing/printing the HTML test report.
  - Understanding the HTML report.
  - Saving test projects.

Contact Agilent

For more information on DDR2 Compliance Test Application or other Agilent Technologies' products, applications and services, please contact your local Agilent office. The complete list is available at:

www.agilent.com/find/contactus

Phone or Fax

United States:

(tel) 800 829 4444

(fax) 800 829 4433

Canada:

(tel) 877 894 4414

(fax) 800 746 4866

China:

(tel) 800 810 0189

(fax) 800 820 2816

Europe:

(tel) 31 20 547 2111

Japan:

(tel) (81) 426 56 7832

(fax) (81) 426 56 7840

Korea:

(tel) (080) 769 0800

(fax) (080) 769 0900

Latin America:

(tel) (305) 269 7500

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(tel) 0800 047 866

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(fax) (65) 6755 0042

E-mail: tm_ap@agilent.com

Contents

4 Single-Ended Signals AC Input Parameters Tests

1 Installing the DDR2 Compliance Test Application

If you purchased the N5413A DDR2 Compliance Test Application separately, you need to install the software and license key.

Installing the Software

1 Make sure you have version A.05.20 or higher of the Infiniium oscilloscope software by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the DDR2 Compliance Test Application, go to Agilent website: http://www.agilent.com/find/N5413A.

3 The link for DDR2 Compliance Test Application will appear. Double-click on it and follow the instructions to download and install the application software.

Installing the License Key

1 Request a license code from Agilent by following the instructions on the Entitlement Certificate.

You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.

2 After you receive your license code from Agilent, choose **Utilities>Install Option License...**.

3 In the Install Option License dialog, enter your license code and click **Install License**.

4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.

5 Click **Close** to close the Install Option License dialog.

6 Choose **File>Exit**.

7 Restart the Infiniium oscilloscope application software to complete the license installation.

2 Preparing to Take Measurements

Before running the DDR2 automated tests, you should calibrate the oscilloscope and probe. No test fixture is required for this DDR2 application. After the oscilloscope and probe have been calibrated, you are ready to start the DDR2 Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

If you haven't already calibrated the oscilloscope and probe, see Chapter 14, "Calibrating the Infiniium Oscilloscope and Probe".

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Agilent recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DDR2 Compliance Test Application

1 Ensure that the RAM reliability test software is running in the computer system where the Device Under Test (DUT) is attached. This software performs tests to all unused RAM in the system by producing a repetitive burst of read-write data signals to the DDR2 memory.

2 To start the DDR2 Compliance Test Application: From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>DDR2 Test**.

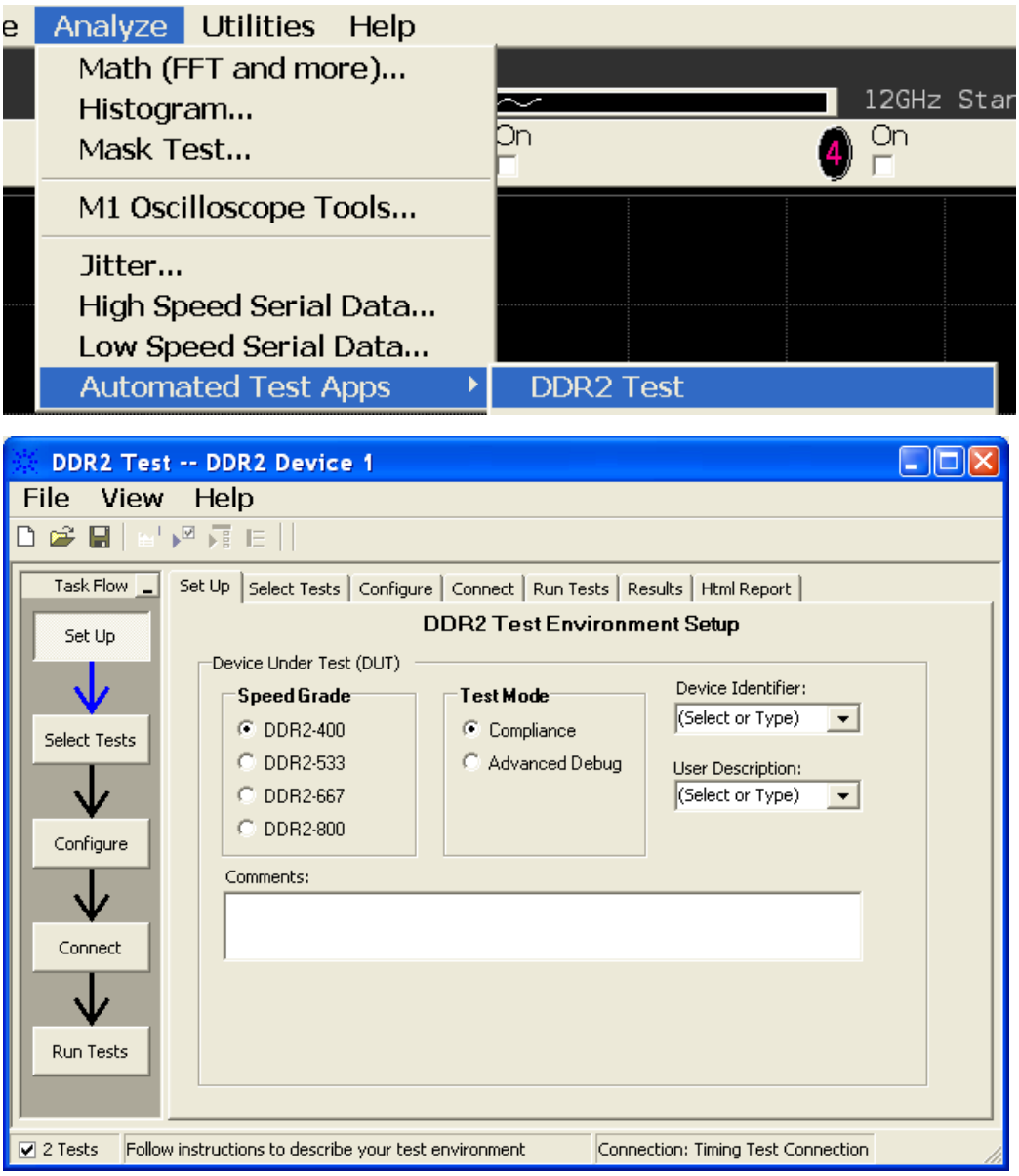

Figure 3 The DDR2 Compliance Test Application

NOTE If DDR2 Test does not appear in the Automated Test Apps menu, the DDR2 Compliance Test Application has not been installed (see Chapter 1, "Installing the DDR2 Compliance Test Application").

Figure 3 shows the DDR2 Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Set Up	Lets you identify and setup the test environment, including information about the device under test.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

NOTE When you close the DDR2 application, each channel's probe is configured as single-ended or differential depending on the last DDR2 test that was run.

Online Help Topics

For information on using the DDR2 Compliance Test Application, see its online help (which you can access by choosing Help>Contents... from the application's main menu).

The DDR2 Compliance Test Application's online help describes:

- Starting the DDR2 Automated Test Application.
  - To view or minimize the task flow pane.
  - To view or hide the toolbar.
- Creating or opening a test project.
- Setting up DDR2 test environment.
- Selecting tests.
- Configuring selected tests.
- Connecting the oscilloscope to the Device Under Test (DUT).
- Running tests.
- Viewing test results.
  - To show reference images and flash mask hits.
  - To change margin thresholds.
- Viewing/printing the HTML test report.
- Understanding the HTML report.
- Saving test projects.

3 Measurement Clock Tests

This section provides the Methods of Implementation (MOIs) for Rising Edge and Pulse Measurements Clock tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Measurement Clock Tests

When performing the Measurement Clock tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connections for Rising Edge and Pulse Measurement Clock tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

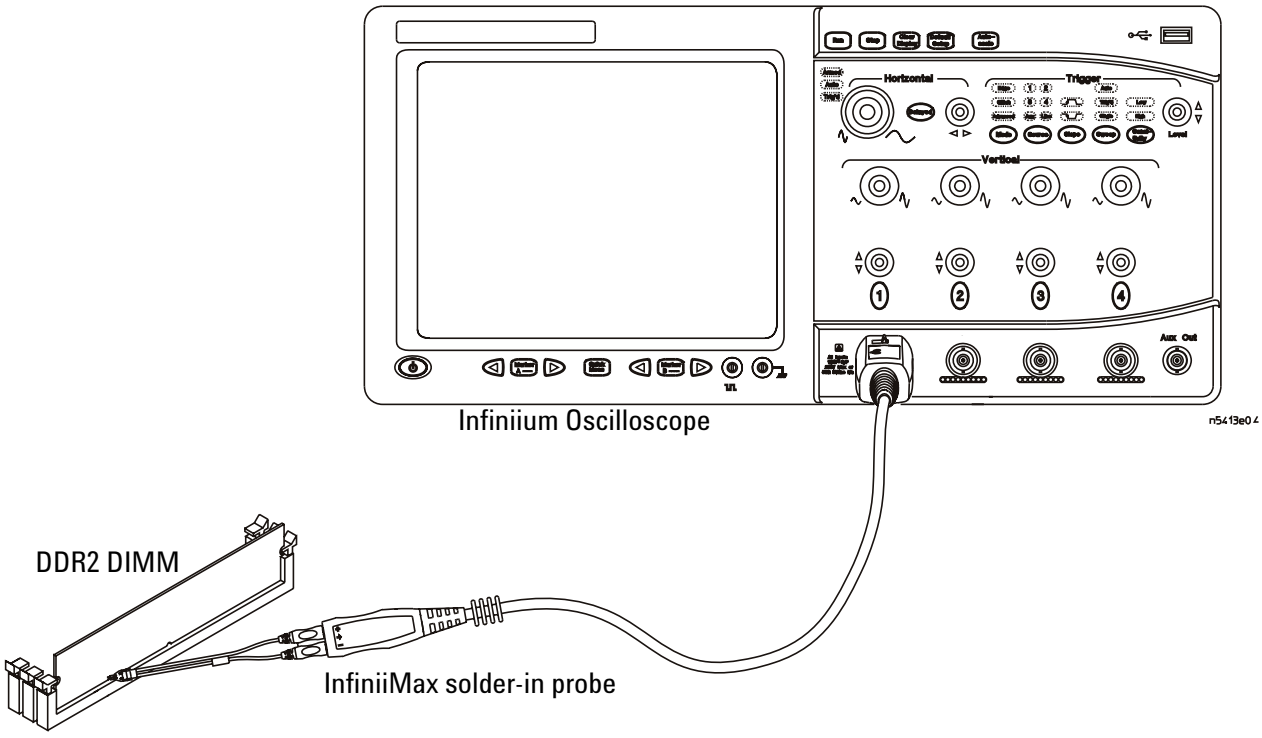

Figure 4 Probing for Measurement Clock Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channel shown in Figure 4 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUT on the DDR2 DIMM.
4. Connect the oscilloscope probes to any of the oscilloscope channels.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For the DDR2 Measurement Clock tests, you can select either DDR2-667 or DDR2-800. If other Speed Grade is selected, the Measurement Clock test options will not be displayed at the Select tab.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

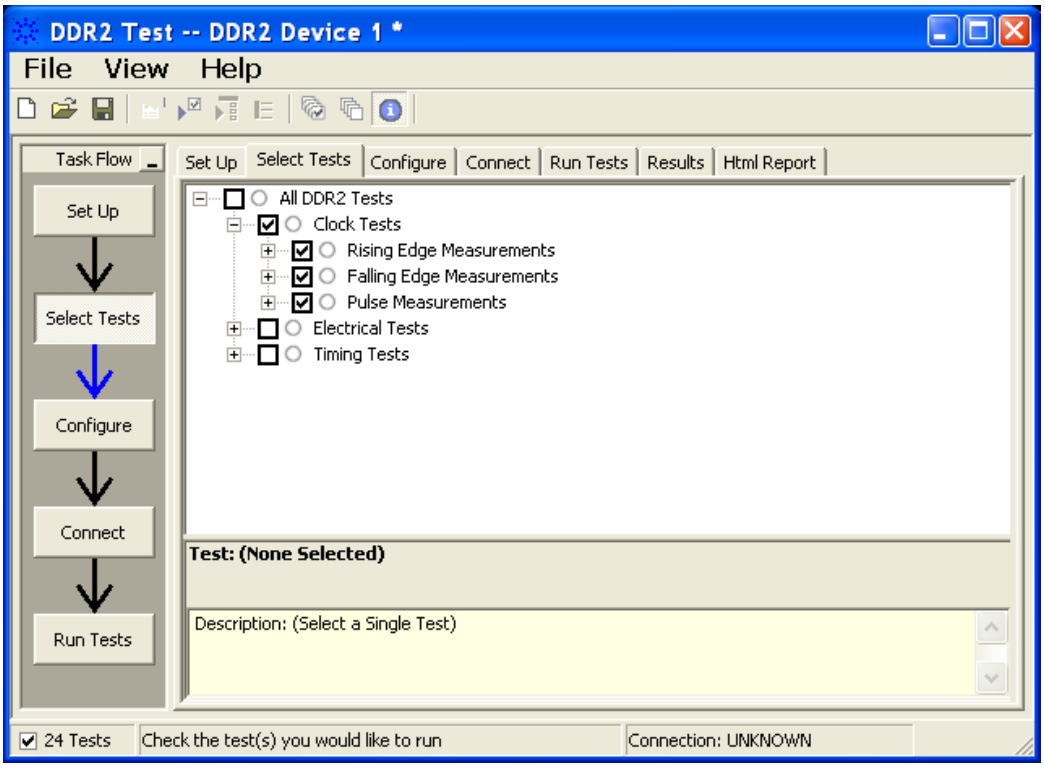

Figure 5 Selecting Measurement Clock Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 4), run the test, and view the test results.

Table 4 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(dc)	Input voltage high value (direct current).
Vih(ac)	Input voltage high value (alternating current).
Vil(dc)	Input voltage low value (direct current).
Vil(ac)	Input voltage low value (alternating current).
Waveform Source	Identifies the source of the data to be analyzed.
Use Recommended Memory Depth	Sets the Memory Depth to the maximum recommended value. Select "No" if you plan to manually select the memory depth.
Use Fixed Sampling Rate and Bandwidth	Sets the Sampling Rate to 20 GSa and Bandwidth to AUTO. Select "No" if you plan to manually select sampling rate or bandwidth settings.
Worst Case Tracking	
Mark Worst Case Cycle	Places markers around the worst case cycles (test-dependent).
terr(nper) SubWindow Range	
terr(nper) Minimum N Width Value	Sets the lower bound (inclusive) of the inner sliding window for the terr(nper) series.
terr(nper) Maximum N Width Value	Sets the upper bound (inclusive) of the inner sliding window for the terr(nper) series.

Clock Period Jitter - tJIT(per) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement and Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock. You can specify the rising and/or the falling edge of your signal for this measurement.

Signals of Interest

Based on the test definition (Read cycle only):

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 5 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Clock Period Jitter	tJIT(per)	-125	125	-100	100	ps	

Pass Condition

The tJIT(per) measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1.*

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures the difference between every period inside a 200 cycle window with the average of the whole window.
2. Compare periods with the new average.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Cycle to Cycle Period Jitter - tJIT(cc) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as Falling Edge Measurement. The purpose of this test is to measure the difference in the clock period between two consecutive clock cycles. The tJIT(cc) Rising Edge Measurement measures the clock period from the rising edge of a clock cycle to the next rising edge. The tJIT(cc) Falling Edge Measurement measures the clock period from the falling edge to falling edge. The test will show a fail status if the total failed waveforms is greater than 0.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 6 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Cycle to Cycle Period Jitter	tJIT(cc)	-250	250	-200	200	ps	

Pass Condition

The tJIT(cc) measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the difference between every adjacent pair of periods.
2. Generate 201 measurement results.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Cumulative Error - tERR(n per) - Test Method of Implementation

This Cumulative Error (across “n” cycles) test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. The purpose of this test is to measure the difference between a measured clock period and the average clock period across multiple cycles of the clock.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user’s speed grade selection

Test Definition Notes from the Specification

Table 7 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units
		min	max	min	max	
Cumulative error across 2 cycles	tERR(2per)	-175	175	-150	150	ps
Cumulative error across 3 cycles	tERR(3per)	-225	225	-175	175	ps
Cumulative error across 4 cycles	tERR(4per)	-250	250	-200	200	ps
Cumulative error across 5 cycles	tERR(5per)	-250	250	-200	200	ps
Cumulative error across $6 \le n \le 10$ cycles	tERR(6-10)	-600	600	-300	300	ps
Cumulative error across $11 \le n \le 50$ cycles	tERR(11-50)	-600	600	-450	450	ps

Pass Condition

The tERR measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. tERR(2per) is similar to tJIT(per), except it makes a small 2-cycle window inside the big 200 cycle window and compares the average of the small window with the average of the big window.
2. Check the results for the smallest and largest values (worst case values).
3. Compare the results against the compliance test limits.
4. tERR(3per) is the same as tERR(2per) except the small window size is 3 periods wide. tERR(4per) uses small window size of 4 periods and tERR(5per) uses 5 periods.
5. tERR(6-10per) executes tERR(6per), tERR(7per), tERR(8per), tERR(9per) and tERR(10per), combines all the measurement results together into one big pool and checks for the smallest and largest value.
6. tERR(11-50per) does the same for tERR(11per) through tERR(50per).

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Average High Pulse Width - tCH(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the positive pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 8 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	3000	8000	2500	8000	ps	
Average High Pulse Width	tCH(avg)	0.48	0.52	0.48	0.52	tCK(avg)	

Pass Condition

The tCH measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the high pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Average Low Pulse Width - tCL(avg) - Test Method of Implementation

The purpose of this test is to measure the average duty cycle of all the negative pulse widths within a window of 200 consecutive cycles.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 9 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	3000	8000	2500	8000	ps	
Average Low Pulse Width	tCL(avg)	0.48	0.52	0.48	0.52	tCK(avg)	

Pass Condition

The tCL measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. Measure the sliding "window" of 200 cycles.
2. Measure the width of the low pulses (1-200, 2-201 and 3-202) and determine the average value for this window.
3. Check the total 3 results for the smallest and largest values (worst case values).
4. Compare results against the compliance test limits.

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Half Period Jitter - tJIT(duty) - Test Method of Implementation

The Half Period Jitter tJIT(duty) can be divided into tJIT(CH) Jitter Average High and tJIT(LH) Jitter Average Low. The tJIT(CH) Jitter Average High Measurement measures between a positive pulse width of a cycle in the waveform, and the average positive pulse width of all cycles in a 200 consecutive cycle window. tJIT(LH) Jitter Average Low Measurement measures between a negative pulse width of a cycle in the waveform and the average negative pulse width of all cycles in a 200 consecutive cycle window.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 10 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Half period jitter	tJIT(duty)	-125	125	-100	100	ps	

Pass Condition

The tJIT(duty) measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

tJIT(CH)

1. This measurement measures the difference between every high pulse width inside a 200 cycle window with the average of the whole window.
2. Measure the difference between high pulse width, and the average. Save the answer as the measurement result.

3 Compare the high pulse width with the new average.

4 Check the results for the smallest and largest values (worst case values).

5 Compare the test results against the compliance test limits.

tJIT(CH)

1 This measurement is similar to tJIT(CH) above except, instead of using high pulse widths, it uses low pulse widths for testing comparison.

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Average Clock Period - tCK(avg) - Test Method of Implementation

This test is applicable to the Rising Edge Measurement as well as the Falling Edge Measurement. tCK(avg) is average clock period within 200 consecutive cycle window. The tCK(avg) Rising Edge Measurement measures the period from the rising edge of a cycle to the next rising edge within the waveform window. The tCK(avg) Falling Edge Measurements measures from the falling edge to the falling edge.

Signals of Interest

Based on the test definition:

- Clock Signal

Signals required to perform the test on the oscilloscope:

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 11 Clock and Duty Cycle Specifications

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Average clock period	tCK(avg)	3000	8000	2500	8000	ps	

Pass Condition

The tCK(avg) measurement value should be within the conformance limits as specified in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

Measurement Algorithm

Example input test signal: Frequency: 1 KHz, Number of cycles acquired: 202.

1. This measurement measures a sliding "window" of 200 cycles.
2. Calculate the average period value for periods 1-200, 2-201 and 3-202.
3. Check the results for the smallest and largest values (worst case values).
4. Compare the test results against the compliance test limits.

Test References

See Clock and Duty Cycle Specifications in the *Intel DDR2 667/800 JEDEC Specification Addendum Rev1.1*.

4 Single-Ended Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals AC Input tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Single-Ended Signals AC Input Parameters Tests

When performing the Single-Ended Signals AC Input Parameters tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for the Single-Ended Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

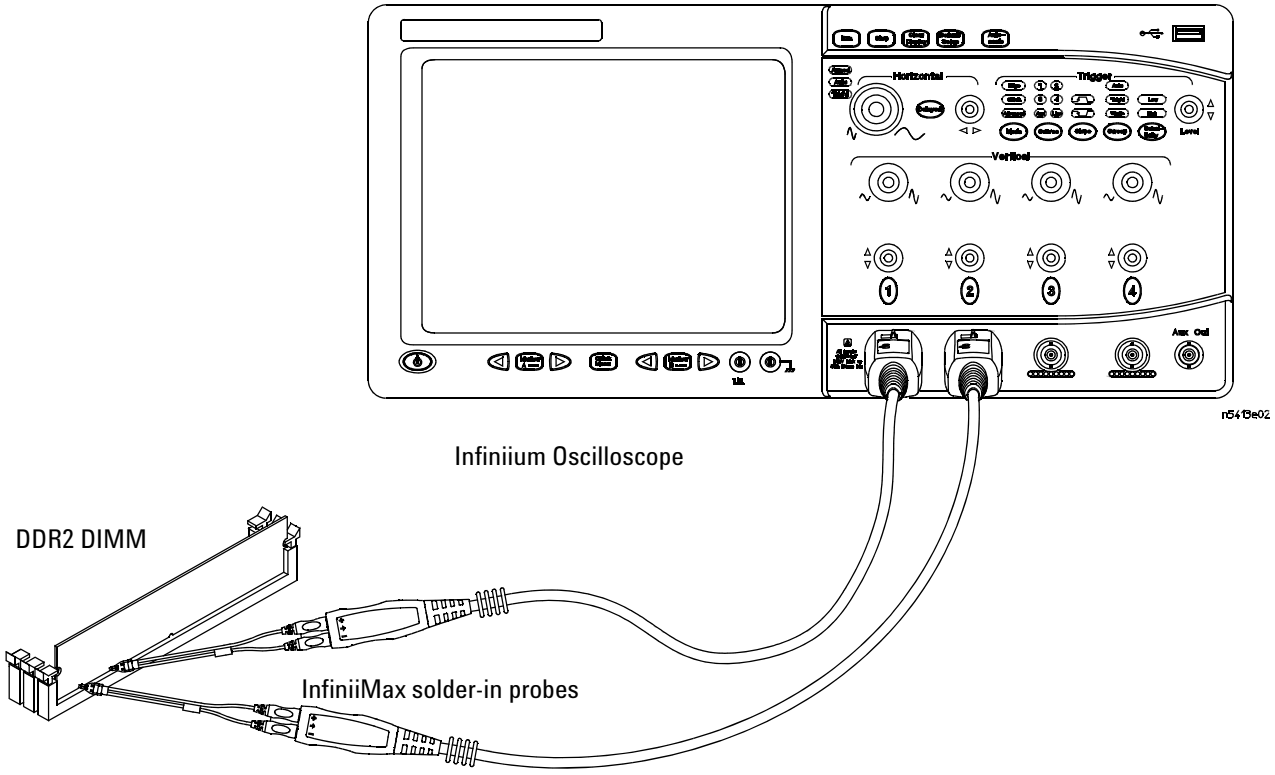

Figure 6 Probing for Single-Ended Signals AC Input Parameters Tests with Two Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 6 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all unused RAM on the system by producing a repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For the Single-Ended Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

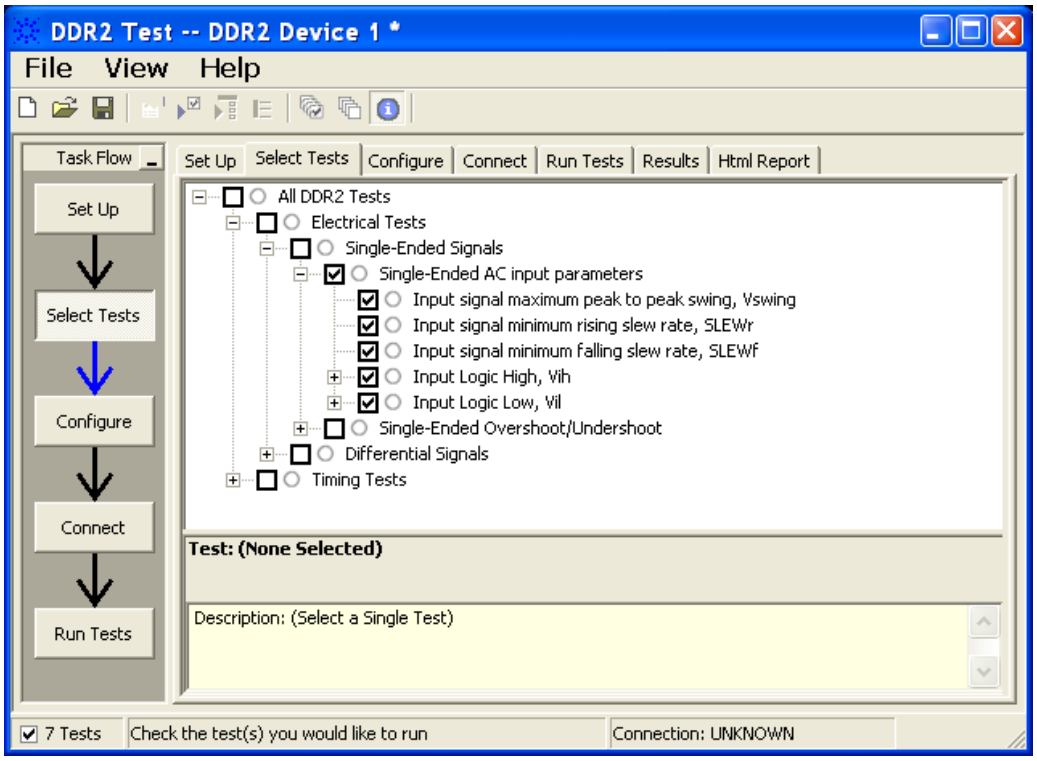

Figure 7 Selecting Single-Ended Signals AC Input Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 12), run the tests and view the tests results.

Table 12 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Single-Ended Signals	
Single-Ended AC Parameters	
Pin Under Test, PUT	Identifies the Pin Under Test for Single-Ended AC parameters.
PUT Source	Identifies the source of the PUT to be analyzed for Single-Ended AC tests.
Supporting Pin	Identifies the required supporting pin for Single-Ended AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Single-Ended AC Tests.

$V_{SWING(MAX)}$ Test Method of Implementation

$V_{SWING(MAX)}$ - Input Signal Maximum Peak To Peak Swing. The purpose of this test is to verify that the peak-to-peak voltage value of the test signal is lower than the conformance maximum limit of the V_{SWING} value specified in the *JEDEC Standard JESD79-2C*.

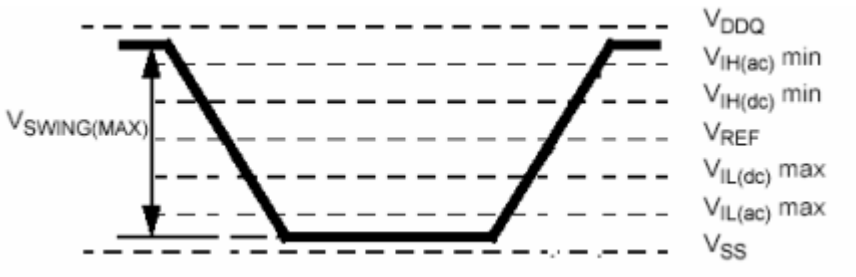

Figure 8 $V_{SWING(MAX)}$

Figure 9 $V_{SWING(MAX)}$ in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Write cycle only):

- Clock Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 13 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1

NOTE 1: Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL(ac)}$ level applied for the device under test.

PASS Condition

$\leq V_{SWING(MAX)}$

The peak-to-peak value for the test signal can be lower than or equal to the $V_{SWING(MAX)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR2 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.

4 Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).

5 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

6 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

7 Setup the required scope settings and histogram function settings.

8 Use histogram 'Peak-to-Peak' value as the test result for V_{SWING}.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for V_{SWING}.

10 Compare test results against the compliance test limit.

Test References

See Table 21 - AC Input test Conditions, in the *JEDEC Standard JESD79-2C*.

$Slew_R$ Test Method of Implementation

$Slew_R$ - Input Signal Minimum Slew Rate (Rising). The purpose of this test is to verify that the rising slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the *JEDEC Standard JESD79-2C*.

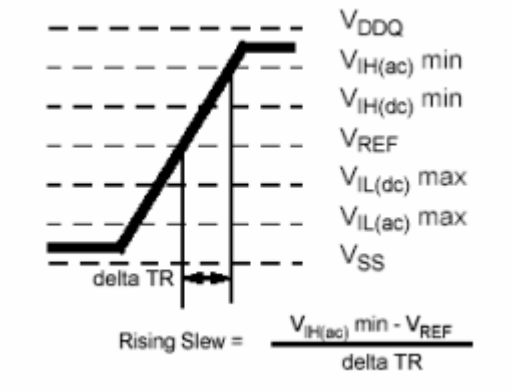

Figure 10 $Slew_R$

Figure 11 $Slew_R$ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 14 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 2: The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$min for falling edges as shown in the above figure.

NOTE 3: AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

PASS Condition

$\geq SLEW_R$

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR2 speed grade.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Verify that V_{REF} and $V_{IH(AC)}$ points can be found on the oscilloscope screen.
9. Calculate the delta TR.
10. Calculate Rising Slew.

$$\mathrm{RisingSlew} = \frac{V_{IH(ac)}\mathrm{min} - V_{REF}}{\Delta TR}$$

11. Compare test results against the compliance test limit.

Test References

See Table 21 - AC Input Test Conditions, in the *JEDEC Standard JESD79-2C*.

$Slew_F$ Test Method of Implementation

$Slew_F$ - Input Signal Minimum Slew Rate (Falling). The purpose of this test is to verify that the falling slew rate value of the test signal is greater than or equal to the conformance limit of the input SLEW value specified in the *JEDEC Standard JESD79-2C*.

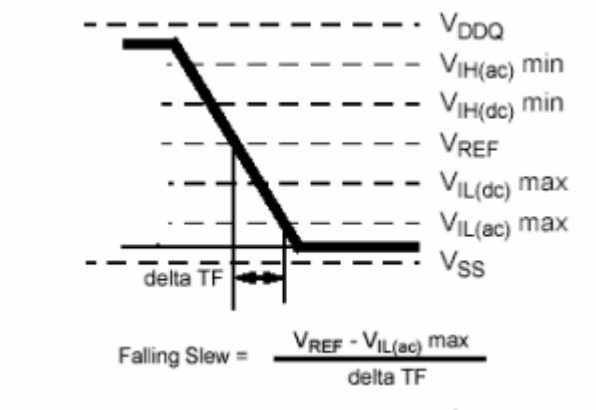

Figure 12 $Slew_F$

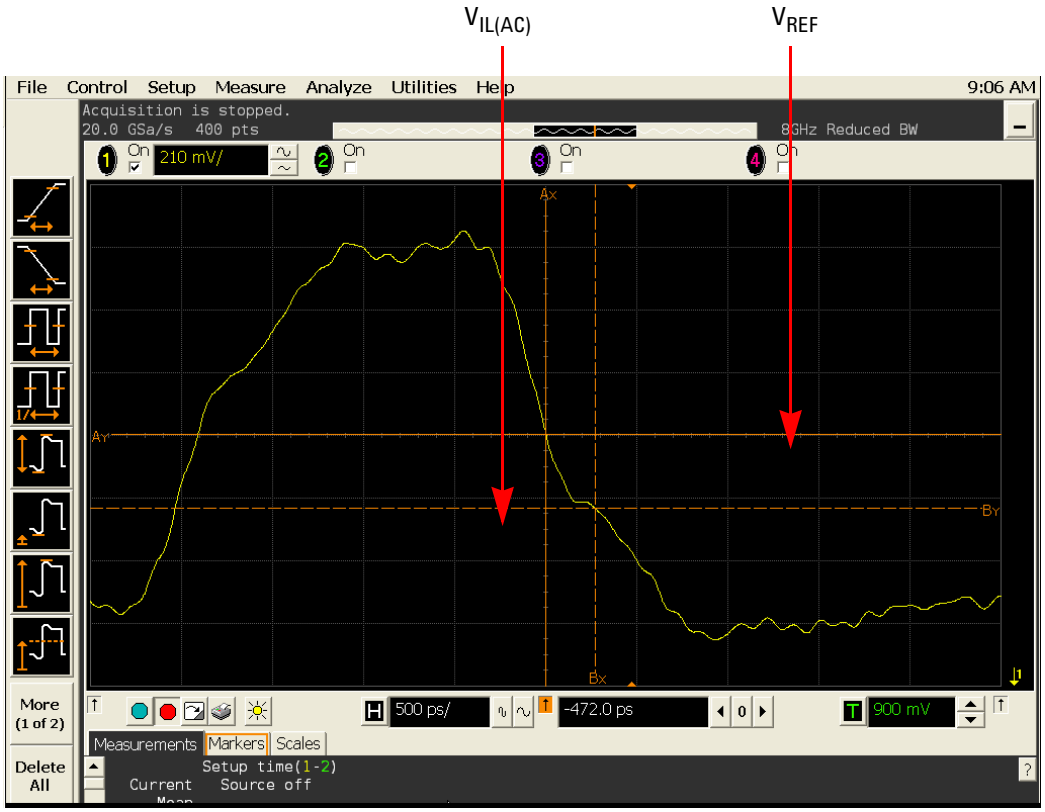

Figure 13 $Slew_F$ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 15 AC Input Test Conditions

Symbol	Condition	Value	Units	Notes
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE 2: The input signal minimum slew rate is to be maintained over the range from V_{REF} to $V_{IH(ac)}$min for falling edges as shown in the above figure.

NOTE 3: AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

PASS Condition

$\geq SLEW_F$

The calculated Rising Slew value for the test signal should be greater than or equal to the SLEW value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR2 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on DQ-DQS to make sure it can be triggered during Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Verify that V_{REF} and $V_{IL(AC)}$ points can be found on the oscilloscope screen.
9. Calculate the delta TR.
10. Calculate the Falling Slew.

$$\text{FallingSlew} = \frac{V_{REF} - V_{IL(ac)}\text{max}}{\Delta TF}$$

11. Compare test results against the compliance test limit.

Test References

See Table 21 - AC Input Test Conditions, in the *JEDEC Standard JESD79-2C*.

$V_{IH(AC)}$ Test Method of Implementation

V_{IH} Input Logic High Test can be divided into two sub tests - $V_{IH(AC)}$ test and $V_{IH(DC)}$ test.

$V_{IH(AC)}$ - Maximum AC Input Logic High. The purpose of this test is to verify that the maximum high level voltage value of the test signal within a valid sampling window is greater than the conformance lower limit of the $V_{IH(AC)}$ value specified in the *JEDEC Standard JESD79-2C*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

Figure 14 $V_{IH(AC)}$ Test - Maximum AC Input Logic High in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 16 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units
		Min	Max	Min	Max	
$V_{IH(ac)}$	ac input logic high	V_{REF} + 0.250	-	V_{REF} + 0.200	-	V

PASS Condition

$\geq V_{IH(ac)}$

The maximum value for the high level voltage should be greater than or equal to the minimum $V_{IH(AC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR2 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Max** value as the test result for $V_{IH(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IH(AC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 20 - Input AC Logic Level, in the *JEDEC Standard JESD79-2C*.

$V_{IH(DC)}$ Test Method of Implementation

$V_{IH(DC)}$ - Minimum DC Input Logic High. The purpose of this test is to verify that the minimum high level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IH(DC)}$ value specified in the *JEDEC Standard JESD79-2C*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value as well.

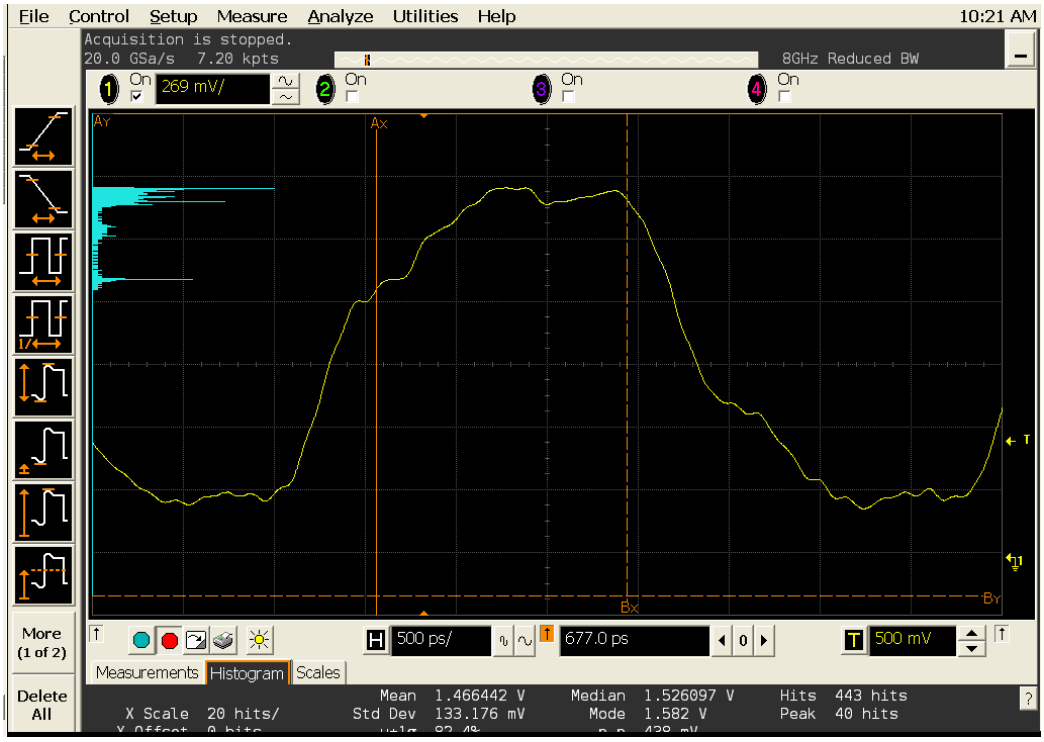

Figure 15 $V_{IH(DC)}$ Test - Minimum DC Input Logic High in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 17 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IH(dc)}$	dc input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V	N/A

PASS Condition

The minimum value for the high level voltage should be greater than or equal to the minimum $V_{IH(DC)}$ value.

The minimum value for the high level voltage should be less than or equal to the maximum $V_{IH(DC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR2 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Min** value as the test result for $V_{IH(DC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IH(DC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2C*.

$V_{IL(AC)}$ Test Method of Implementation

V_{IL} AC Input Logic Low High Test can be divided into two sub tests: $V_{IL(AC)}$ test and $V_{IL(DC)}$ test.

$V_{IL(AC)}$ - Minimum AC Input Logic Low. The purpose of this test is to verify that the minimum low level voltage value of the test signal is lower than the conformance maximum limit of the $V_{IL(AC)}$ value specified in the *JEDEC Standard JESD79-2C*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

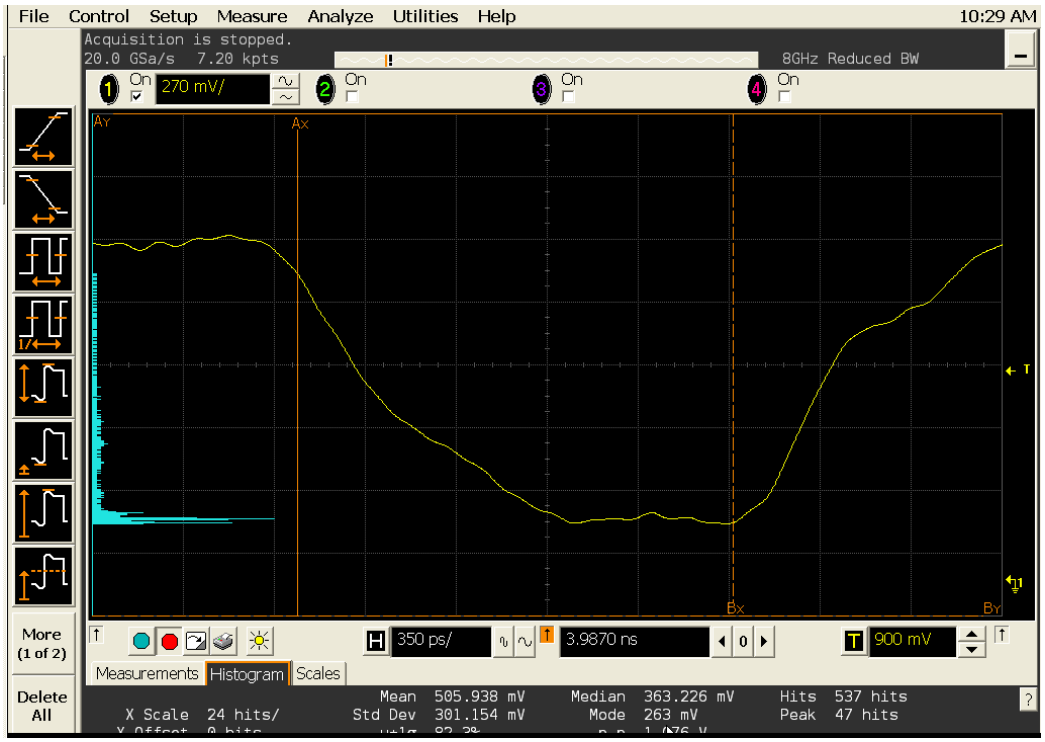

Figure 16 $V_{IL(AC)}$ Test - Minimum AC Input Logic Low in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR

- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 18 Input AC Logic Level

Symbol	Parameter	DDR2-400, DDR2-533		DDR2-667, DDR2-800		Units
		Min	Max	Min	Max	
$V_{IL(ac)}$	ac input logic low	N/A	V_{REF} - 0.250	N/A	V_{REF} - 0.200	V

PASS Condition

$\leq V_{IL(AC)}$

The minimum value for the low level voltage should be less than or equal to the maximum $V_{IL(AC)}$ value.

Measurement Algorithm

1. Calculate initial time scale value based on the selected DDR2 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurements to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Min** value as the test result for $V_{IL(AC)}$.

9 When multiple trials are performed, the largest value (worst case) among the trials will be used as the test result for $V_{IL(AC)}$.

10 Compare test results against the compliance test limits.

Test References

See Table 20 - Input AC Logic Level, in the *JEDEC Standard JESD79-2C*.

$V_{IL(DC)}$ Test Method of Implementation

$V_{IL(DC)}$ - Maximum DC Input Logic Low. The purpose of this test is to verify that the maximum low level voltage value of the test signal within a valid sampling window is within the conformance limits of the $V_{IL(DC)}$ value specified in the *JEDEC Standard JESD79-2C*.

The value of V_{REF} which directly affects the conformance lower limit is defaulted to 0.9 V. However, users have the flexibility to change this value.

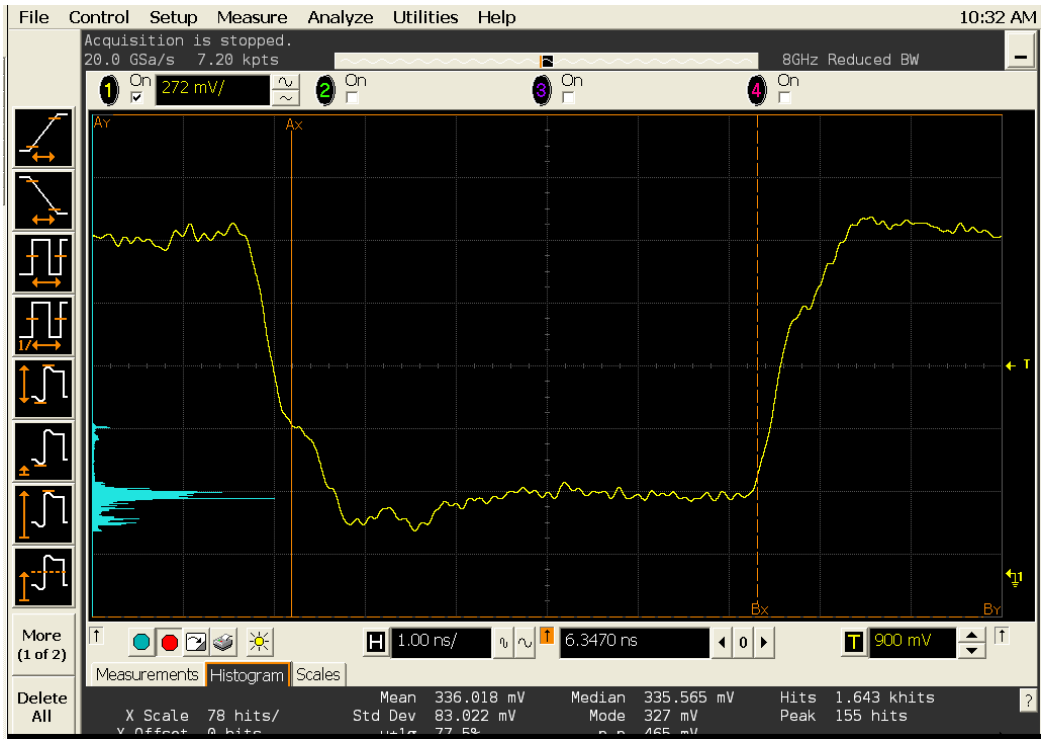

Figure 17 $V_{IL(DC)}$ Test - Maximum DC Input Logic Low in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 19 Input DC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IL(dc)}$	dc input logic low	-0.3	V_{REF} - 0.125	V	N/A

PASS Condition

The maximum value for the low level voltage should be less than or equal to the maximum $V_{IL(DC)}$ value.

The maximum value for the low level voltage should be greater than or equal to the minimum $V_{IL(DC)}$ value.

Measurement Algorithm

1. Calculate the initial time scale value based on the selected DDR2 speed grade options.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate the number of sampling points according to the time scale value.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Setup the required scope settings and histogram function settings.
8. Use the histogram **Max** value as the test result for $V_{IL(DC)}$.
9. When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for $V_{IL(DC)}$.
10. Compare test results against the compliance test limits.

Test References

See Table 19 - Input DC Logic Level, in the *JEDEC Standard JESD79-2C*.

5 Single-Ended Signals Overshoot/Undershoot Tests

This section provides the Methods of Implementation (MOIs) for Single-Ended Signals Overshoot/Undershoot tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Overshoot/Undershoot Tests

When performing the Single-Ended Signals Overshoot/Undershoot tests, the DDR2 Compliance Test Application will prompt you to make the proper connections as shown in the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

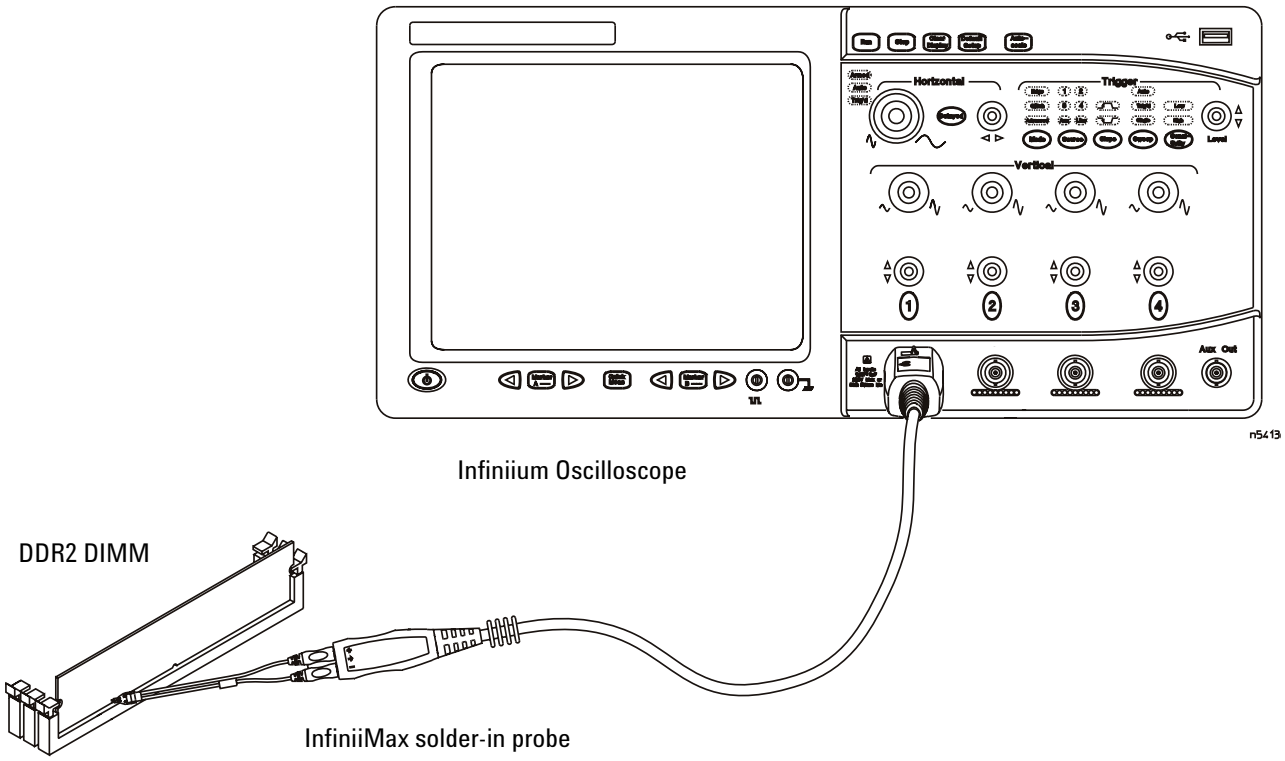

Figure 18 Probing for Single-Ended Signals Overshoot/Undershoot Tests

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channel shown in Figure 18 is just an example).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Single-Ended Signals Overshoot/Undershoot tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

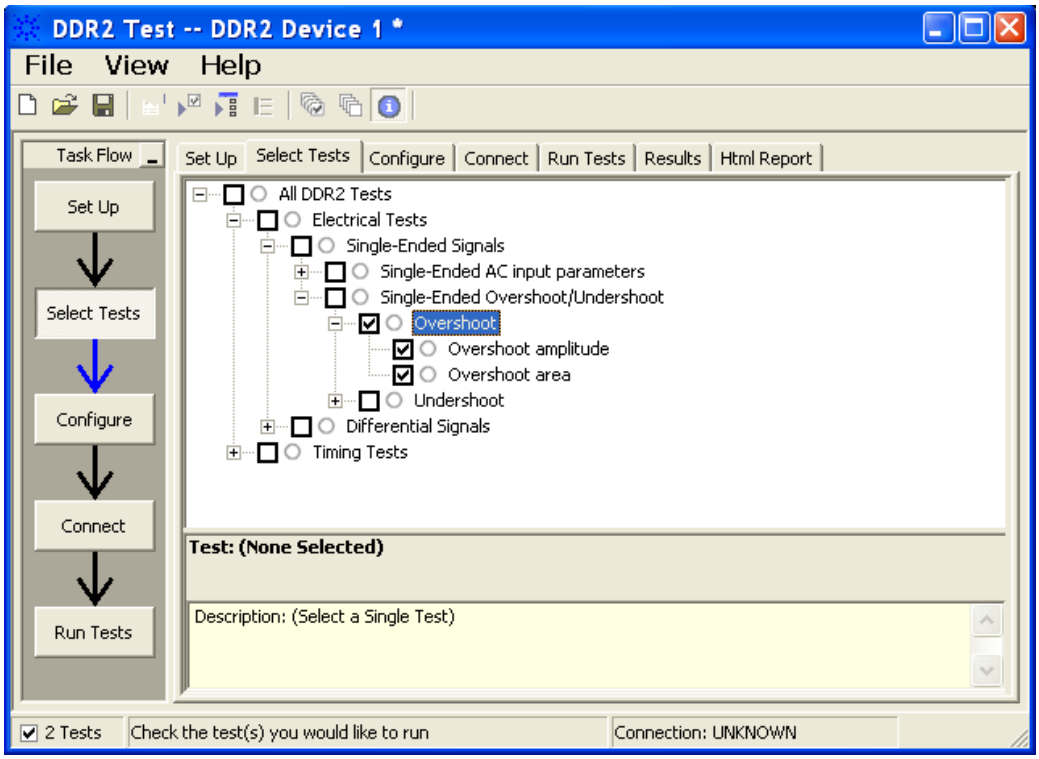

Figure 19 Selecting Single-Ended Signals Overshoot/Undershoot Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 20), run the tests and view the tests results.

Table 20 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Single-Ended Signals	
Single-Ended Overshoot/Undershoot	
Pin Under Test, PUT	Identifies the Pin Under Test for Single-Ended Overshoot/Undershoot.
PUT Source	Identifies the source of the PUT to be analyzed for Single-Ended AC tests.

AC Overshoot Test Method of Implementation

The Overshoot test can be divided into two sub-tests: Overshoot amplitude and Overshoot area. The purpose of this test is to verify that the overshoot value of the test signal is lower than or equal to the conformance limit of the maximum peak amplitude allowed for overshoot as specified in the *JEDEC Standard JESD79-2C*.

When there is an overshoot, the area is calculated based on the overshoot width. The Overshoot area should be lower than or equal to the conformance limit of the maximum Overshoot area allowed as specified in the *JEDEC Standard JESD79-2C*.

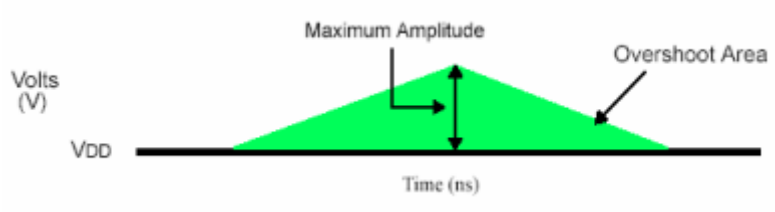

Figure 20 AC Overshoot

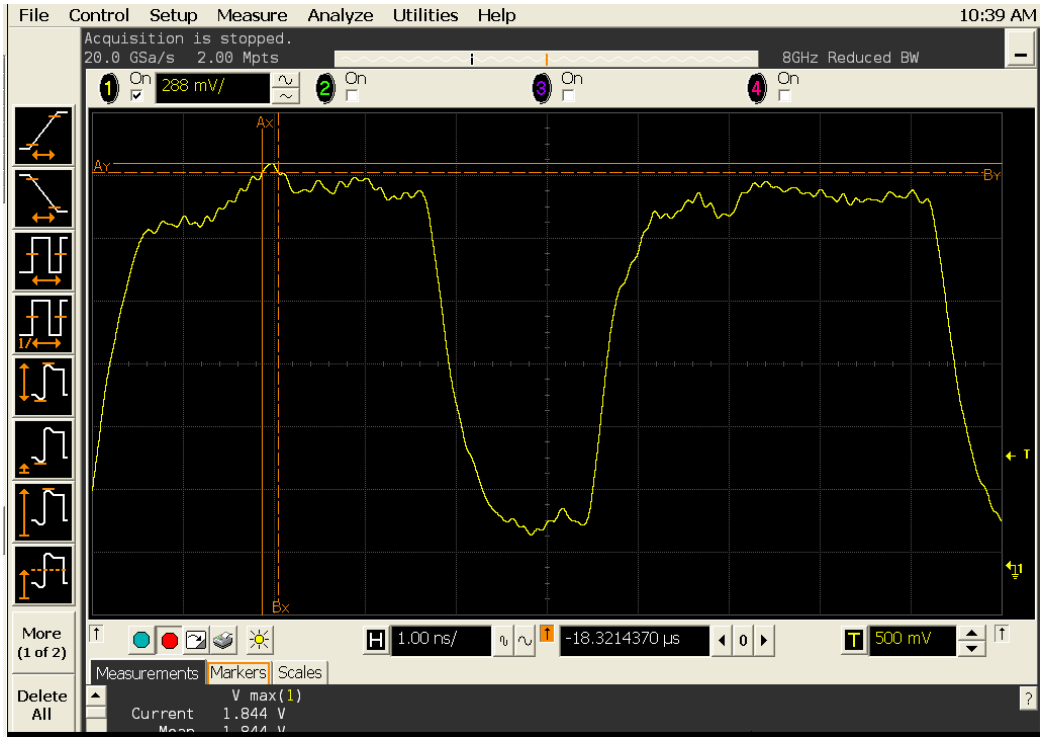

Figure 21 AC Overshoot in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 21 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum overshoot area above VDD	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns

NOTE 1: The maximum requirements for peak amplitude were reduced from 0.9 V to 0.5 V. Register vendor data sheets will specify the maximum overshoot/undershoot induced in specific RDIMM applications. DRAM vendor data sheets will also specify the maximum overshoot/undershoot that their DRAM can tolerate. This will allow the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register will induce in the specific RDIMM application.

Table 22 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

DQ, (U/L/R)DQS, $\overline{\text{(U/L/R)DQS}}$, DM, CK, $\overline{\text{CK}}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for overshoot area	0.5 V	0.5 V	0.5 V	0.5 V
Maximum overshoot area above VDDQ	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

PASS Condition

The measured maximum voltage value can be less than or equal to the maximum overshoot value.

The calculated Overshoot area value can be less than or equal to the maximum Overshoot area allowed.

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate initial time scale value based on the number of sampling points.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Initialize the scope settings.
8. Get timestamp of maximum peak voltage on the waveform.
9. Perform manual zoom waveform to maximum peak area.
10. Get the timestamp of voltage value for VDD(-1.8 V) level closest to the peak point value in order to calculate the maximum overshoot length duration.

11 Calculate the Overshoot area (V-ns)

   a Area of calculation is based on the area of calculation of a triangle where the Overshoot width is used as the triangle base and the Overshoot amplitude is used as the triangle height.

   b Area = 0.5 * base * height.

12 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for the Overshoot amplitude and Overshoot area. The worst case for the area might not happen during the worst case for the amplitude.

13 Compare test results against the compliance test limits.

Test References

See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins, in the *JEDEC Standard JESD79-2C*.

See Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79-2C*.

AC Undershoot Test Method of Implementation

The Undershoot Test can be divided into two sub-tests: Undershoot amplitude and Undershoot area. The purpose of this test is to verify that the undershoot value of the test signal is less than or equal to the conformance limit of the maximum peak amplitude allowed for undershoot as specified in the *JEDEC Standard JESD79-2C*.

When there is an undershoot, the area is calculated based on the undershoot width. The Undershoot area should be less than or equal to the conformance limit of the maximum undershoot area allowed as specified in the *JEDEC Standard JESD79-2C*.

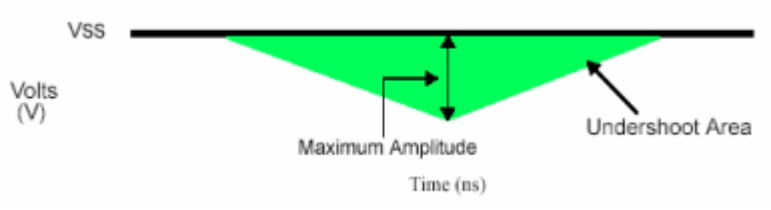

Figure 22 AC Undershoot

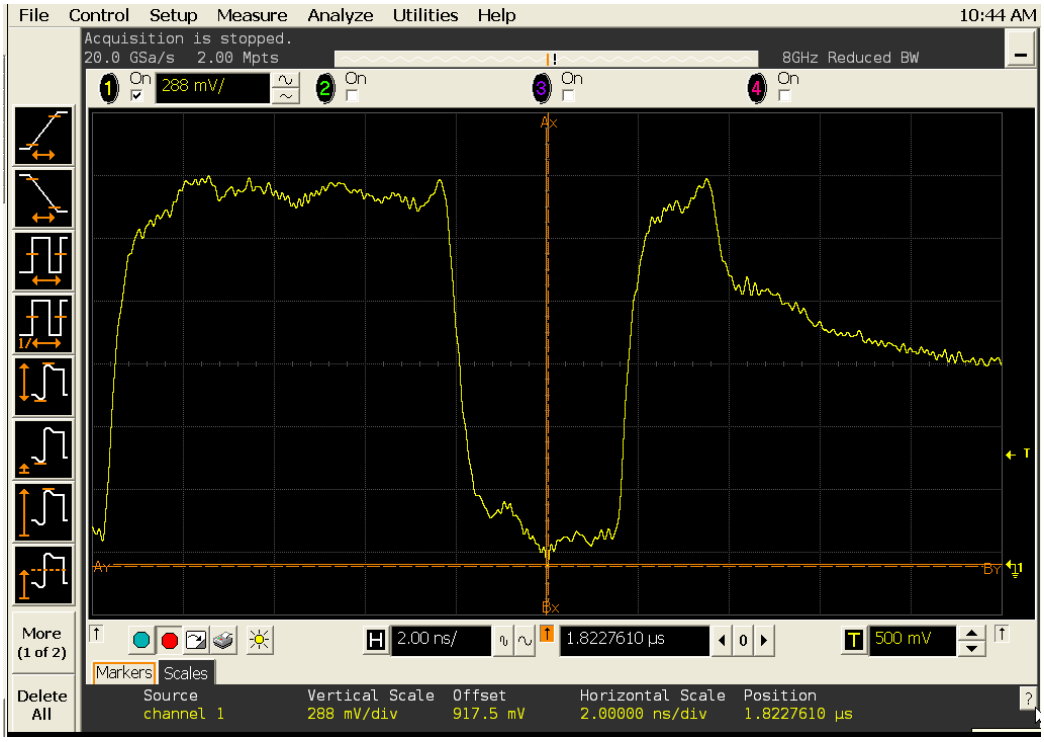

Figure 23 AC Undershoot in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal
- Data Strobe Signal OR
- Address Signal OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)*
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 23 AC Overshoot/Undershoot Specification for Address and Control Pins

A0-A15, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for undershoot area	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V	0.5(0.9)[1] V
Maximum undershoot area above VDD	1.33 V-ns	1.0 V-ns	0.8 V-ns	0.66 V-ns

NOTE 1: The maximum requirements for peak amplitude were reduced from 0.9 V to 0.5 V. Register vendor data sheets will specify the maximum overshoot/undershoot induced in specific RDIMM applications. DRAM vendor data sheets will also specify the maximum overshoot/undershoot that their DRAM can tolerate. This will allow the RDIMM supplier to understand whether the DRAM can tolerate the overshoot that the register will induce in the specific RDIMM application.

Table 24 AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins

DQ, (U/L/R)DQS, $\overline{\text{(U/L/R)DQS}}$, DM, CK, $\overline{\text{CK}}$

Parameter	Specification			
	DDR2-400	DDR2-533	DDR2-667	DDR2-800
Maximum peak amplitude allowed for undershoot area	0.5 V	0.5 V	0.5 V	0.5 V
Maximum undershoot area above VDDQ	0.38 V-ns	0.28 V-ns	0.23 V-ns	0.23 V-ns

PASS Condition

The measured minimum voltage value for the test signal can be less than or equal to the maximum undershoot value.

The calculated undershoot area value can be less than or equal to the maximum undershoot area allowed.

Measurement Algorithm

1. Set the number of sampling points to 2M samples.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Calculate initial time scale value based on the number of sampling points.
4. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
5. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
6. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
7. Initialize the scope settings.
8. Get timestamp of minimum peak voltage on the waveform.
9. Perform manual zoom waveform to minimum peak area.
10. Get timestamp of voltage value for GND (0 V) level closest to the minimum peak point value in order to calculate the undershoot length duration.

11 Calculate the Undershoot area (V-ns)

   a Area of calculation is based on the area of calculation of a triangle where the undershoot width is used as the triangle base and the undershoot amplitude is used as the triangle height.

   b Area = 0.5 * base * height.

12 When multiple trials are performed, the largest value (worst case) among all the trials will be used as the test result for the Undershoot amplitude and Undershoot area. The worst case for the area might not happen during the worst case for the amplitude.

13 Compare test results against the compliance test limits.

Test References

See Table 24 - AC Overshoot/Undershoot Specification for Address and Control Pins, in the *JEDEC Standard JESD79-2C*.

See Table 25 - AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask Pins, in the *JEDEC Standard JESD79-2C*.

6 Differential Signals AC Input Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Input tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Differential Signals AC Input Parameters Tests

When performing the Differential Signals AC Input Parameters tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for the Differential Signals AC Input Parameters tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

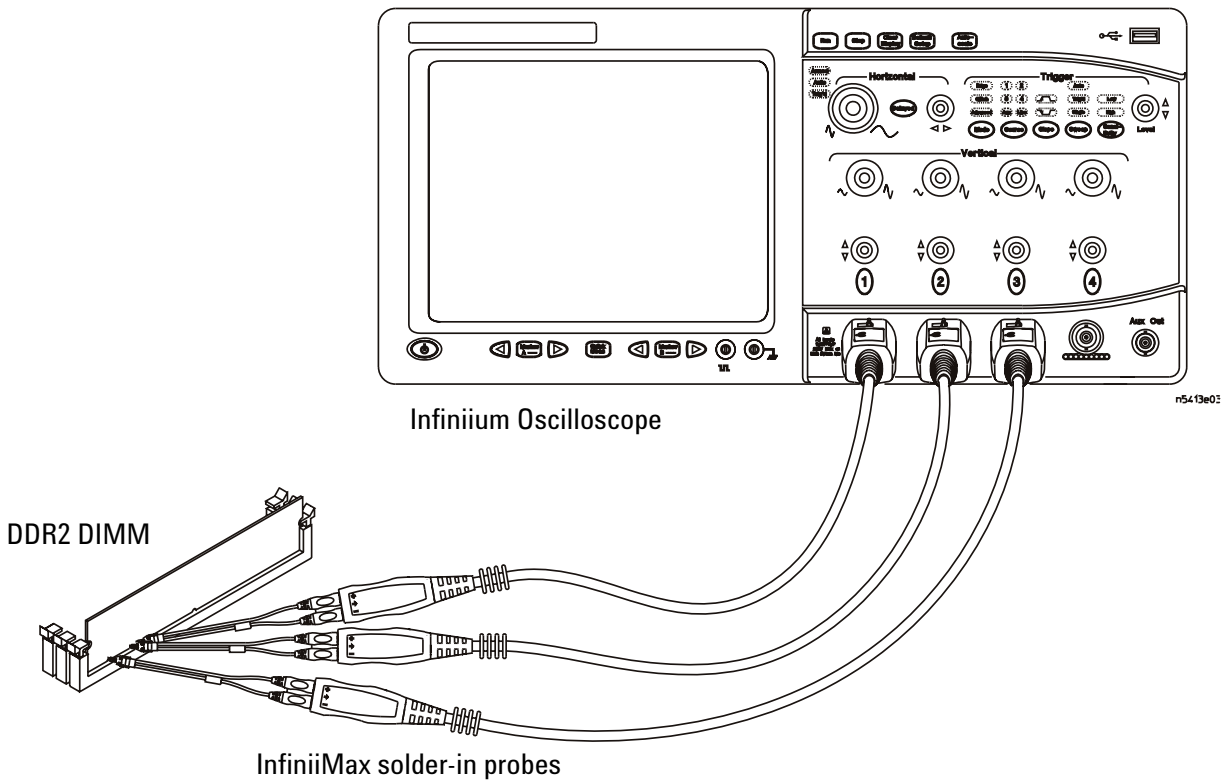

Figure 24 Probing for Differential Signals AC Input Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 24 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Differential Signals AC Input Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

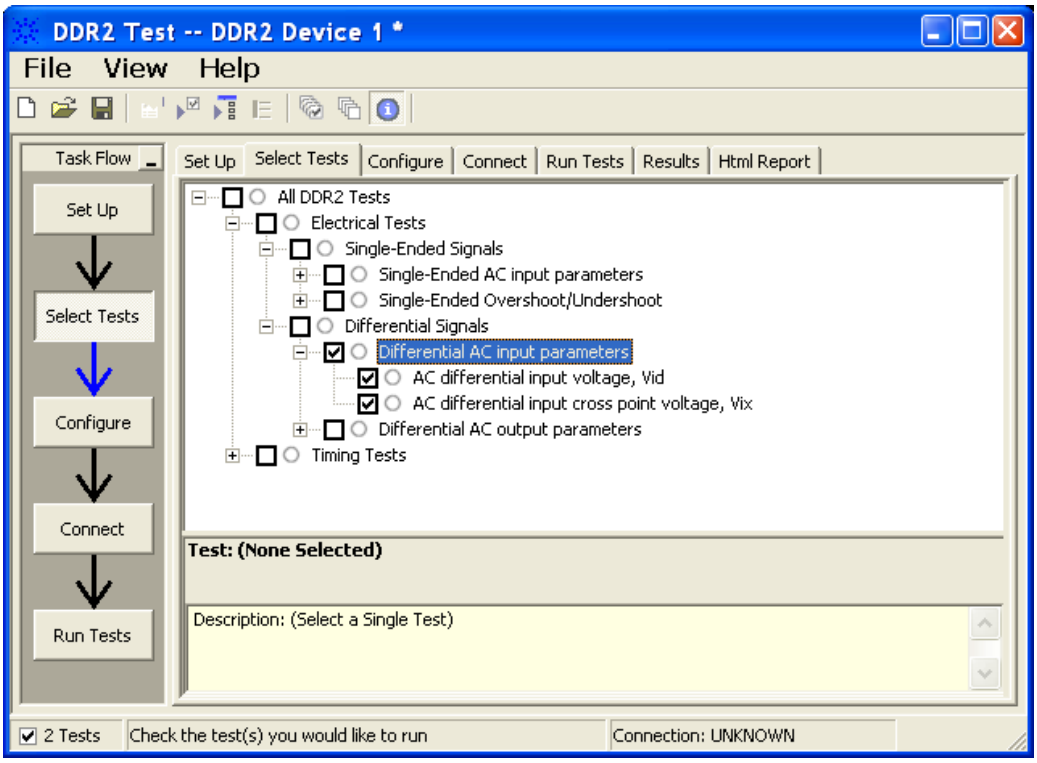

Figure 25 Selecting Differential Signals AC Input Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 25), run the tests and view the tests results.

Table 25 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Differential Tests	
Pin Under Test, PUT	Identifies the Pin Under Test for Differential AC parameters.
PUT (+) Source	Identifies the source of the PUT(+) for Differential AC tests.
PUT (-) Source	Identifies the source of the PUT(-) for Differential AC tests.
Supporting Pin	Identifies the required supporting pin for Differential AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Differential AC tests.

$V_{ID(AC)}$, AC Differential Input Voltage - Test Method of Implementation

The purpose of this test is to verify that the magnitude difference between the differential input signals pair is within the conformance limits of the $V_{ID(AC)}$ as specified in the *JEDEC Standard JESD79-2C*.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value.

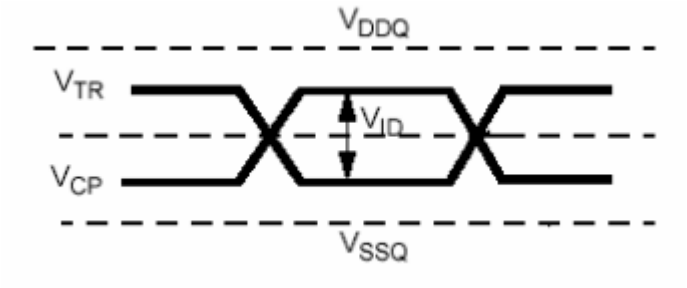

Figure 26 V_{ID} AC Differential Input Voltage

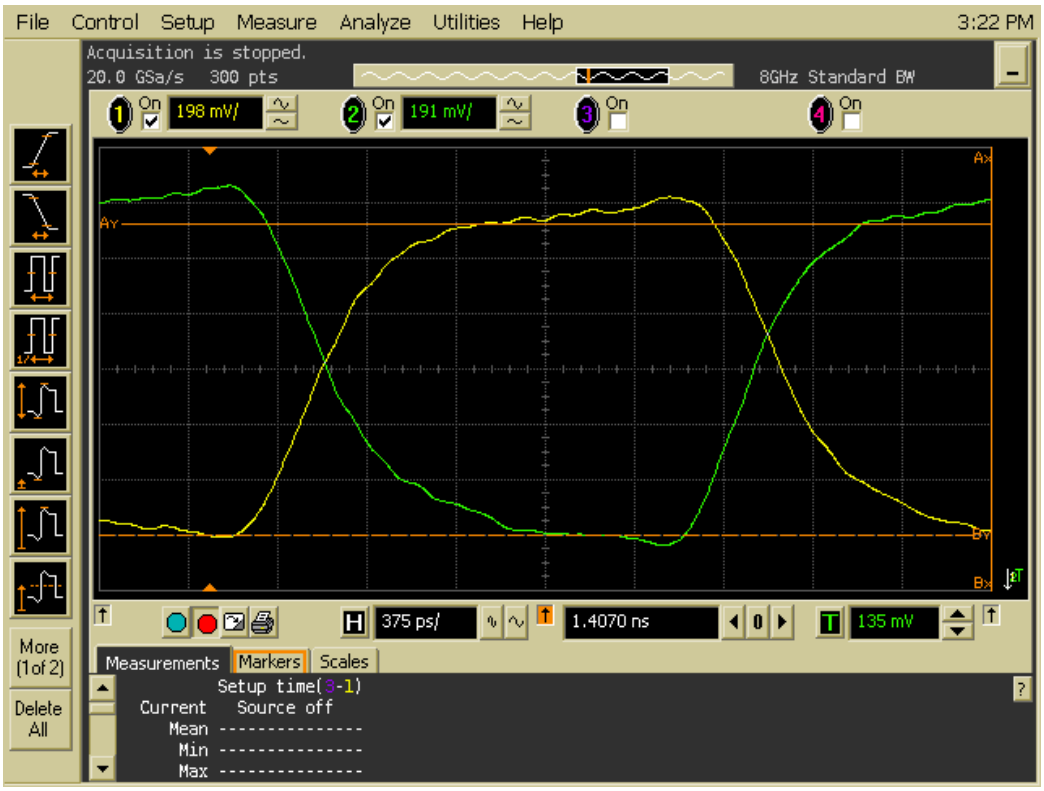

Figure 27 $V_{ID(AC)}$ in Infiniium oscilloscope.

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)*
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 26 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{ID(ac)}$	ac differential input voltage	0.5	V_{DDQ} + 0.6	V	1

NOTE 1: $V_{ID(ac)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where V_{TR} is the true input signal (such as CK, DQS, LDQS or UDQS) and V_{CP} is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to $V_{IH(ac)} - V_{IH(ac)}$.

PASS Condition

The calculated magnitude of the differential voltage for the test signals pair can be within the conformance limits of the $V_{ID(ac)}$ value.

Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Obtain sample or acquire data waveforms, for example CK+ and CK-.

6 Use histogram function (mode value) to find the nominal high level value for CK+ and nominal low level value for CK-.

7 Subtract the CK- low level value from the CK+ high level value.

8 Compare test results against the compliance test limits.

Test References

See Table 22 - AC Input test Conditions, in the *JEDEC Standard JESD79-2C*.

$V_{IX(AC)}$, AC Differential Input Cross Point Voltage -Test Method of Implementation

The purpose of this test is to verify the crossing point of the input differential test signals pair is within the conformance limits of the $V_{IX(AC)}$ as specified in the *JEDEC Standard JESD79-2C*.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value.

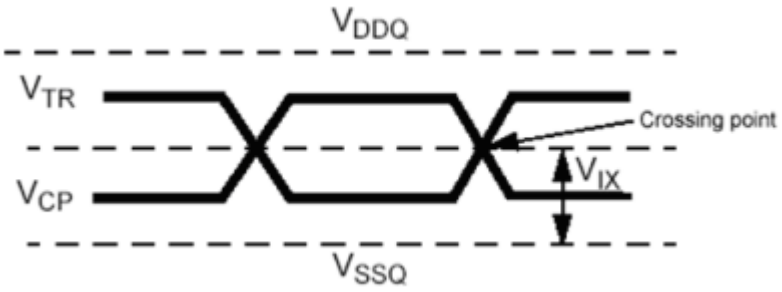

Figure 28 V_{IX} AC Differential Input Voltage

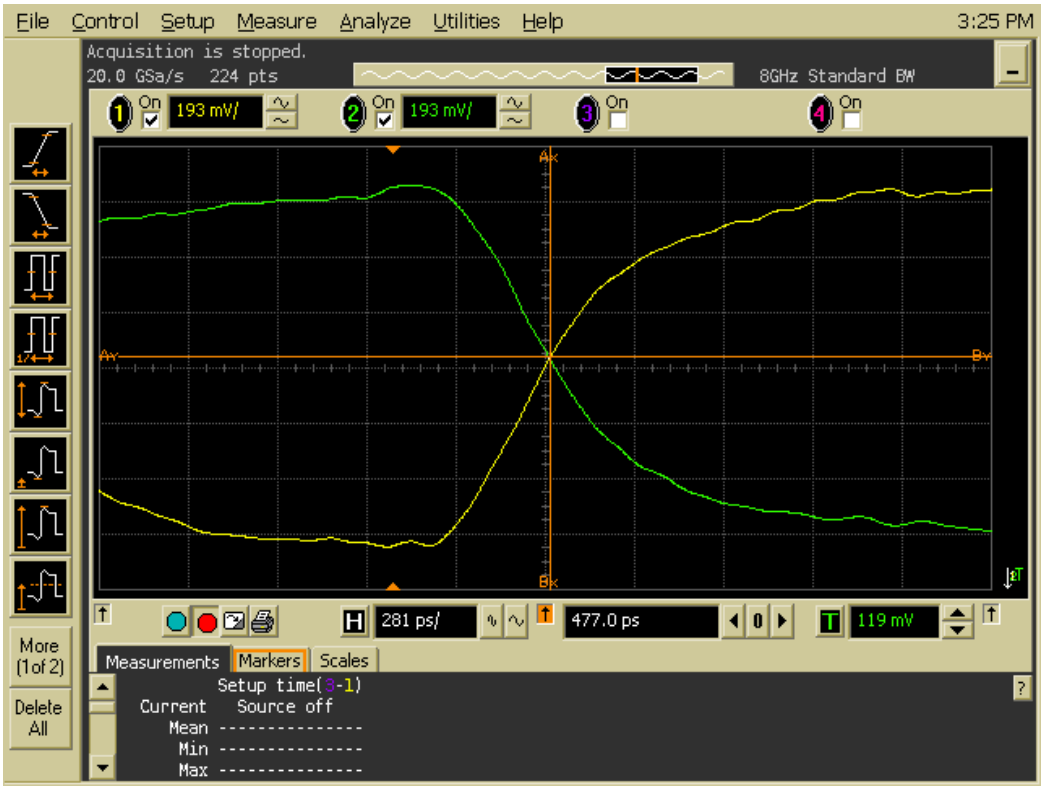

Figure 29 $V_{IX(AC)}$ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal OR
- Clock Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)*
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

* Pin Under Test signal can be either one of the signals under the test definition.

Test Definition Notes from the Specification

Table 27 Differential Input AC Logic Level

Symbol	Parameter	Min	Max	Units	Notes
$V_{IX(ac)}$	ac differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

NOTE 1: The typical value of $V_{IX(ac)}$ is expected to be about 0.5 * V_{DDQ} of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ}. $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.

PASS Condition

The measured crossing point value for the differential test signals pair can be within the conformance limits of $V_{IX(AC)}$ value.

Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Obtain sample or acquire data waveforms, for example CK+ and CK-.

6 Generate the differential waveform from two source input.

7 Get the timestamp of voltage value = 0 V level (crossing point).

8 Get the actual crossing value using the obtained timestamp.

9 Compare test results against the compliance test limits.

Test References

See Table 22 - AC Input Test Conditions, in the *JEDEC Standard JESD79-2C*.

7 Differential Signal AC Output Parameters Tests

This section provides the Methods of Implementation (MOIs) for Differential Signals AC Output tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Differential Signals AC Output Parameters Tests

When performing Differential Signals AC Input Parameters tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Differential Signals AC Output Parameters tests may look similar to below diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance application for the exact number of probe connections.

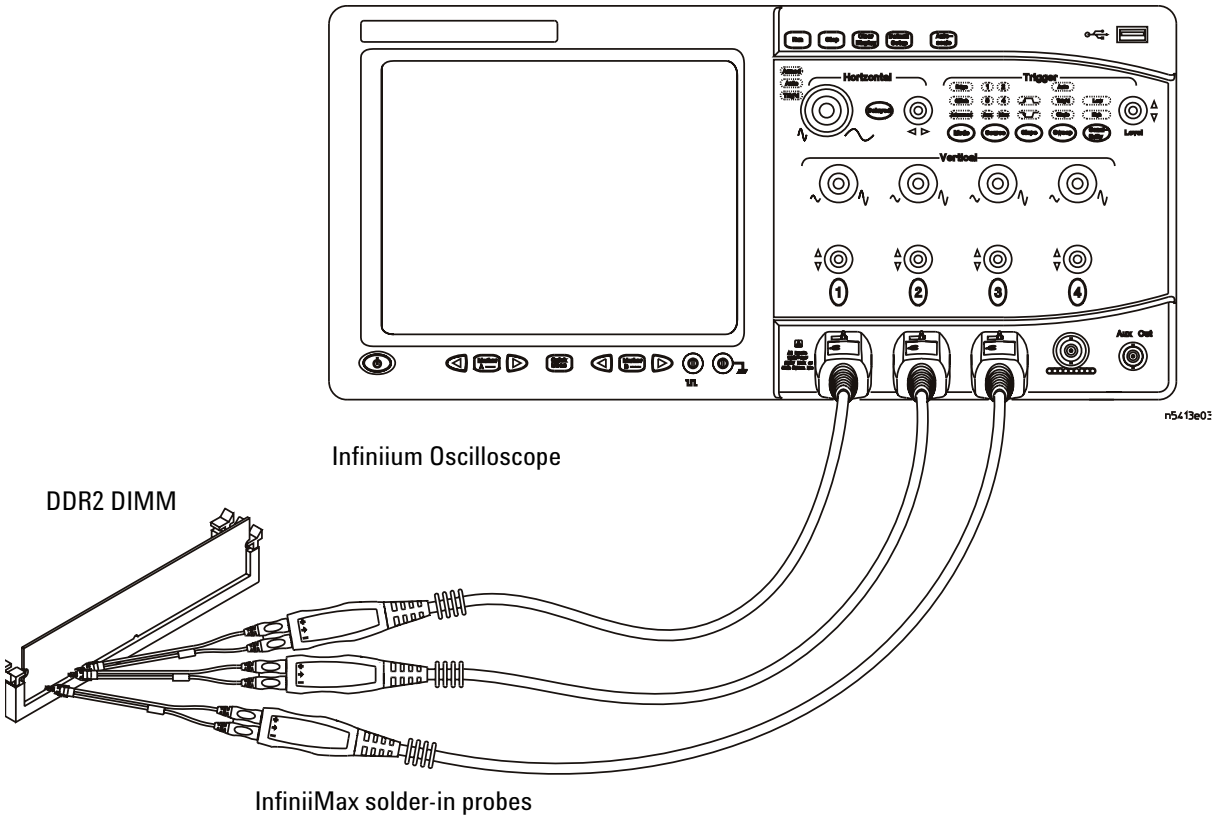

Figure 30 Probing for Differential Signals AC Output Parameters Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 30 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.k
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Differential Signals AC Output Parameters Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

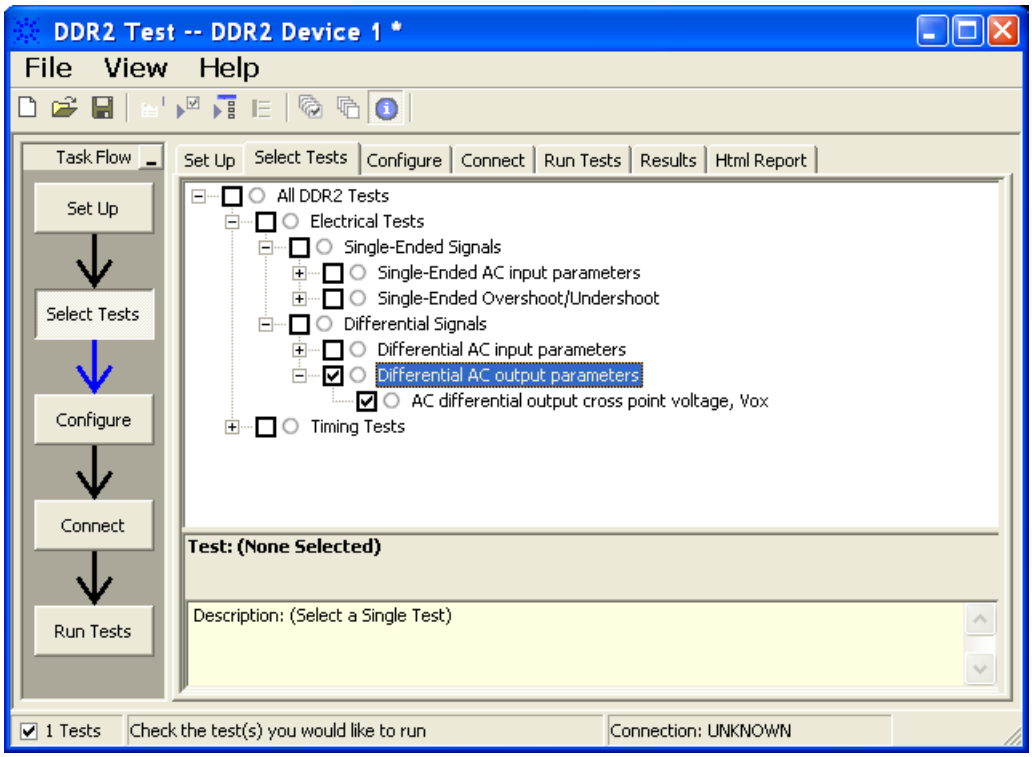

Figure 31 Selecting Differential Signals AC Output Parameters Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 28), run the tests and view the tests results.

Table 28 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle)
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle)
Differential Tests	
Pin Under Test, PUT	Identifies the Pin Under Test for Differential AC parameters.
PUT (+) Source	Identifies the source of the PUT(+) for Differential AC tests.
PUT (-) Source	Identifies the source of the PUT(-) for Differential AC tests.
Supporting Pin	Identifies the required supporting pin for Differential AC parameters.
Supporting Pin Source	Identifies the source of the supporting pin for Differential AC tests.

V_{OX}, AC Differential Output Cross Point Voltage - Test Method of Implementation

The purpose of this test is to verify the crossing point of the output differential test signals pair is within the conformance limits of the $V_{OX(ac)}$ as specified in the *JEDEC Standard JESD79-2C*.

The value of V_{DDQ} which directly affects the conformance upper limit is defaulted to 1.8 V. However, users have the flexibility to change this value.

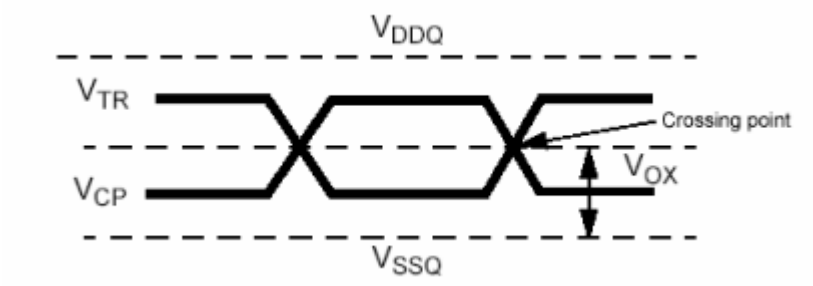

Figure 32 V_{OX} AC Differential Cross Point Voltage

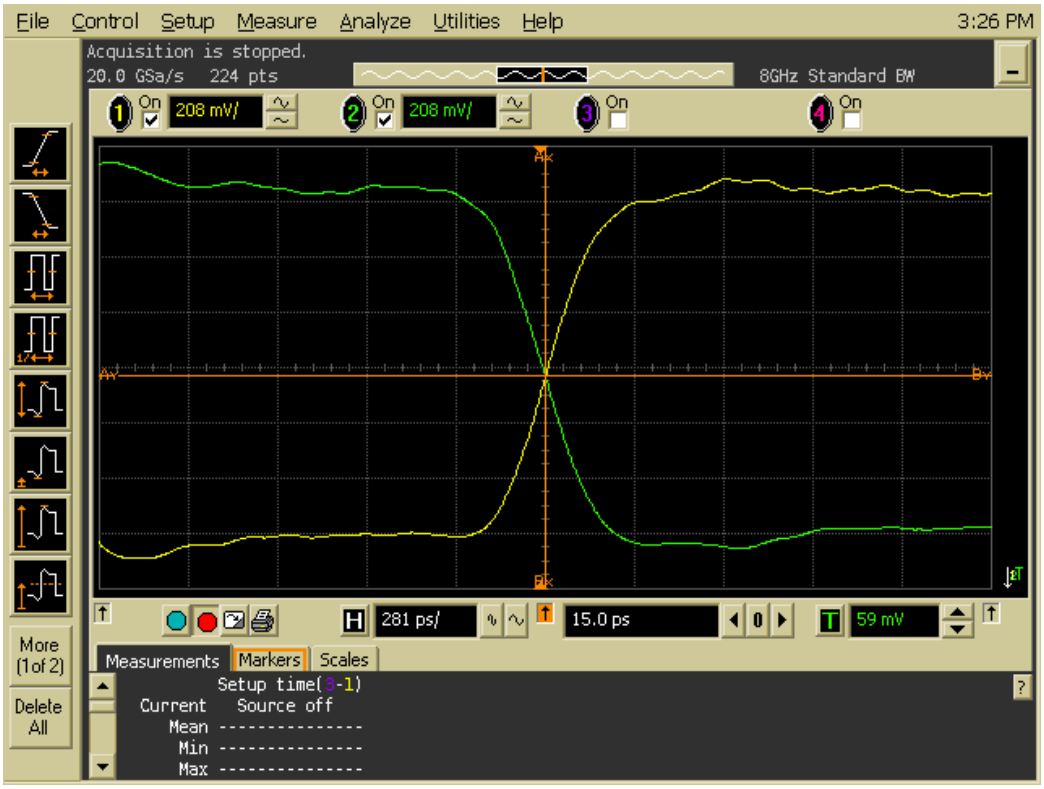

Figure 33 V_{OX} in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Test Definition Notes from the Specification

Table 29 Differential AC Output Parameters

Symbol	Parameter	Min	Max	Units	Notes
$V_{OX(ac)}$	ac differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

NOTE 1: The typical value of $V_{OX(ac)}$ is expected to be about 0.5 * V_{DDQ} of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ}. $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

PASS Condition

The measured crossing point value for the differential test signals pair can be within the conformance limits of $V_{OX(ac)}$ value.

Measurement Algorithm

1. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
2. Obtain sample or acquire signal data and perform signal conditioning to maximize the screen resolution (vertical scale adjustment).
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Obtain sample or acquire data waveforms, for example CK+ and CK-.
6. Generate the differential waveform from two source input.
7. Get the timestamp of voltage value = 0 V level (crossing point).
8. Get the actual crossing value using the obtained timestamp.

9 Compare test results against the compliance test limits.

Test References

See Table 23 - AC Input Test Conditions, in the *JEDEC Standard JESD79-2C*.

8 Clock Timing (CT) Tests

This section provides the Methods of Implementation (MOIs) for Clock Timing tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Clock Timing Tests

When performing the Clock Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Clock Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

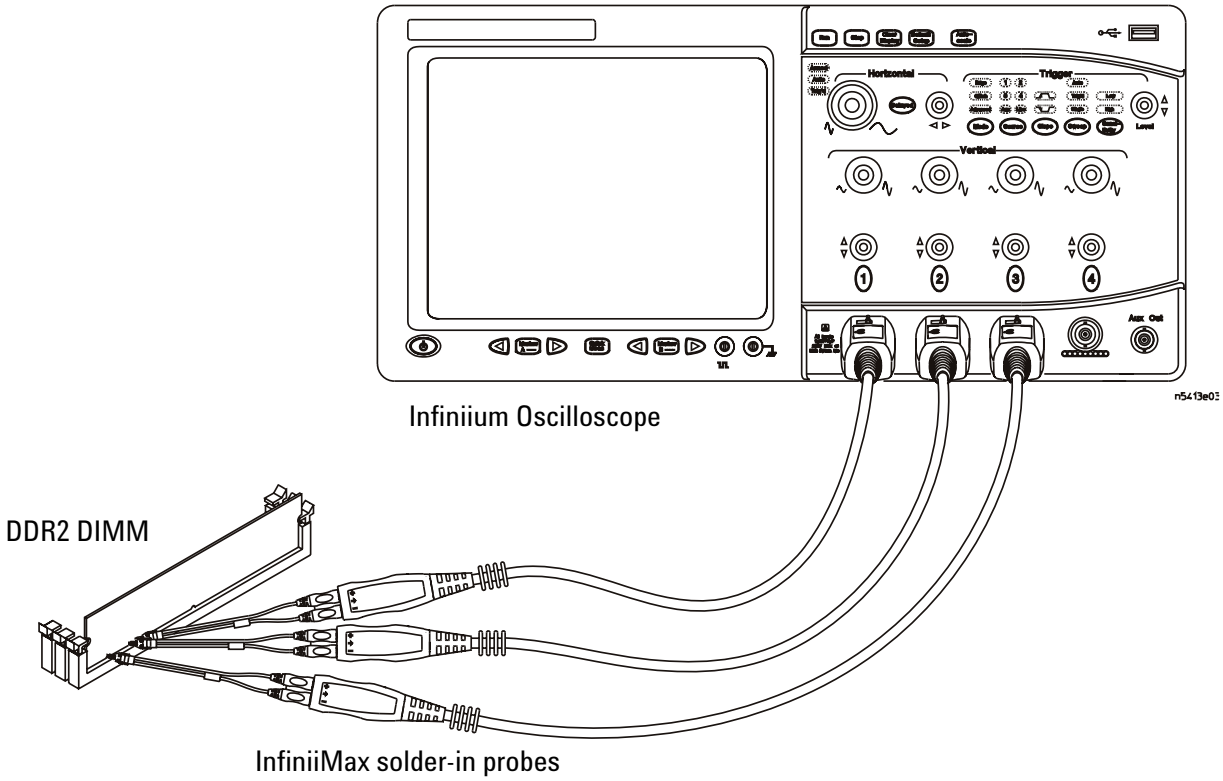

Figure 34 Probing for Clock Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 34 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

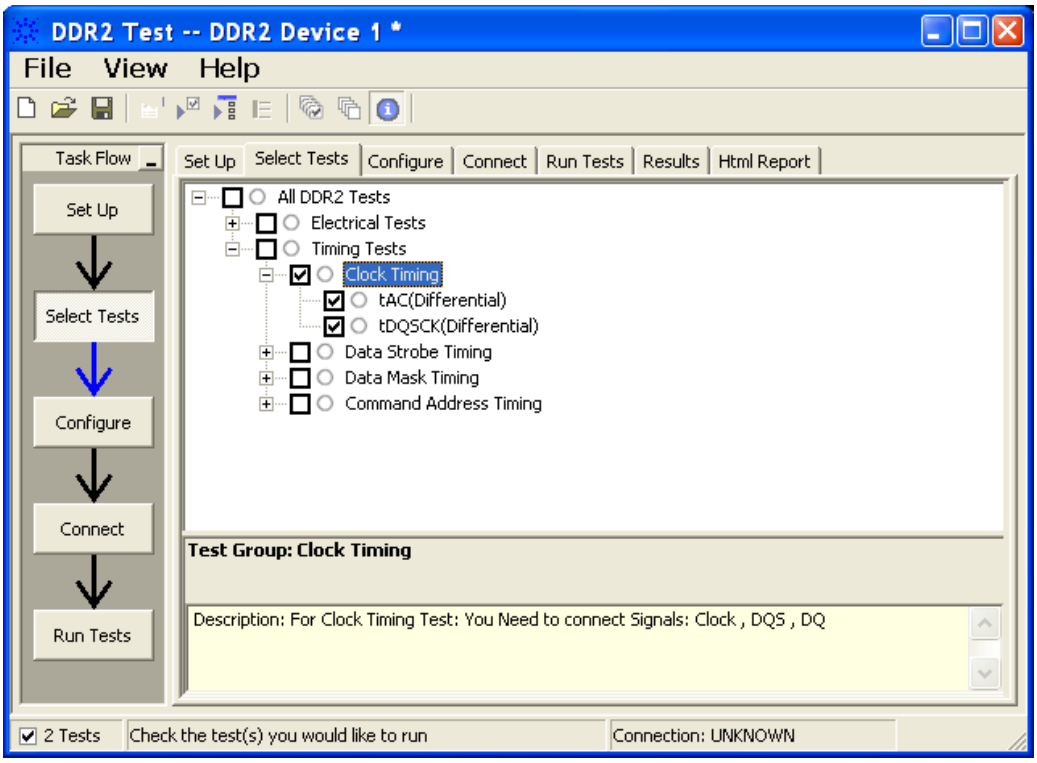

Figure 35 Selecting Clock Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 30), run the tests and view the tests results.

Table 30 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Verify Selected Rank Only?	If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tAC, DQ Output Access Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time interval from data output (DQ Rising and Falling Edge) access time to the nearest rising or falling edge of the clock must be within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

There is tAC(min) and tAC(max) as shown in Figure 36. From the specification, you can observe that the minimum value is at negative while the maximum is at positive.

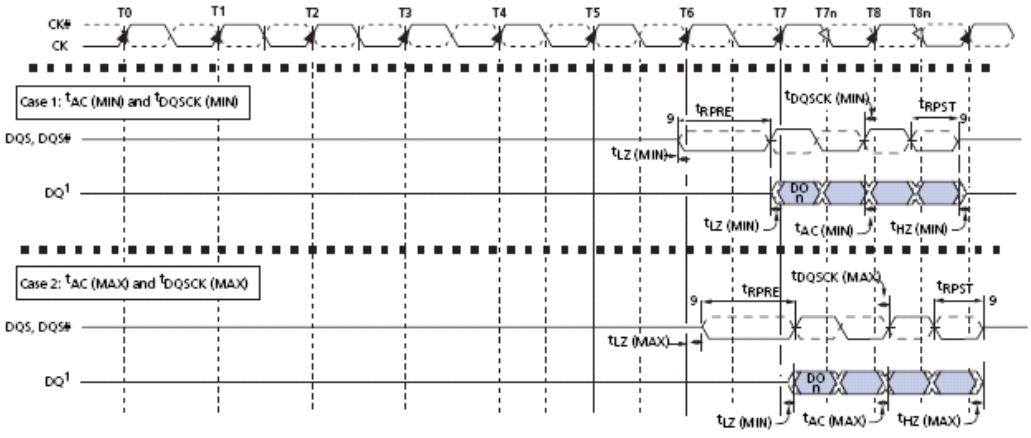

Figure 36 DQ Output Access Time from CK/CK#

Figure 37 tAC in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel

Test Definition Notes from the Specification

Table 31 DQ Output Access Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-600	+600	-500	+500	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ output access time from CK/$\overline{CK}$	tAC	-450	450	-400	400	ps	40

NOTE 40: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min =- 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min -tERR(6-10per), max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max -tERR(6-10),min = 400 ps. + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ), min(derated) = -900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!).

PASS Condition

The measured time interval between the data access output and the rising edge of the clock should be within the specification limits.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.Search for the DQS pre-amble towards the

left from the point where the Read Cycle was previously captured. The For loops, TEdge and DeltaTime are used to search the pre-amble.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge# for the respective signal, begin the tAC measurement bit by bit in Read Data Burst. Begin at the 1st bit of the Read cycle, from the Read pre-amble.

11 Continue the measurement until last bit (for example, until a tristate happens, which indicates the end of a Data Burst for the respective Read Cycle).

12 DQ-Clock timing measurement compares the Rising Edge (Vih_ac OR Vil_dc against clock crossing) OR the Falling Edge (Vil_ac OR Vih_dc against clock crossing).

13 Within the data burst, measure each bit, for instance rising and falling edge of DQ-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for clock signal while marker B for data signal, for the Worst Case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDQSCK, DQS Output Access Time from CK/CK #- Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the nearest rising or falling edge of the clock is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

There is tDQSCK(min) and tDQSCK(max) as shown in Figure 38. From the specification, you can observe that the minimum value is at negative while the maximum is at positive.

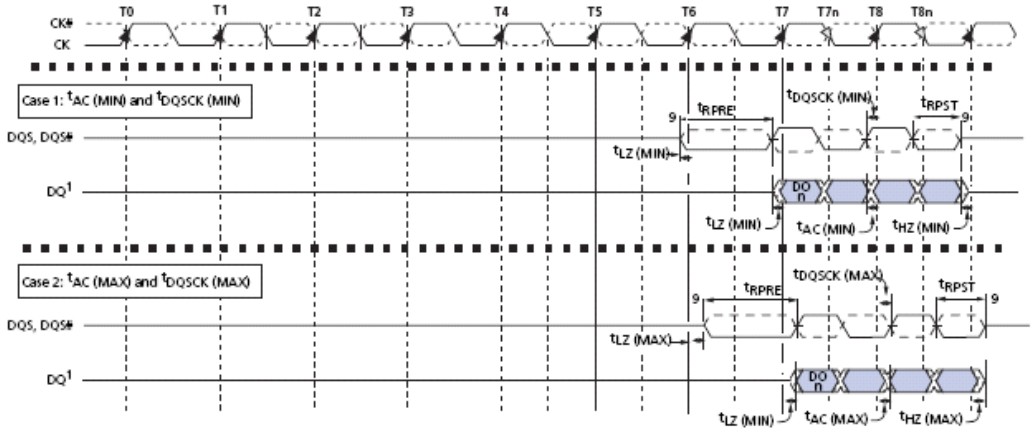

Figure 38 DQS Output Access Time from CK/CK#

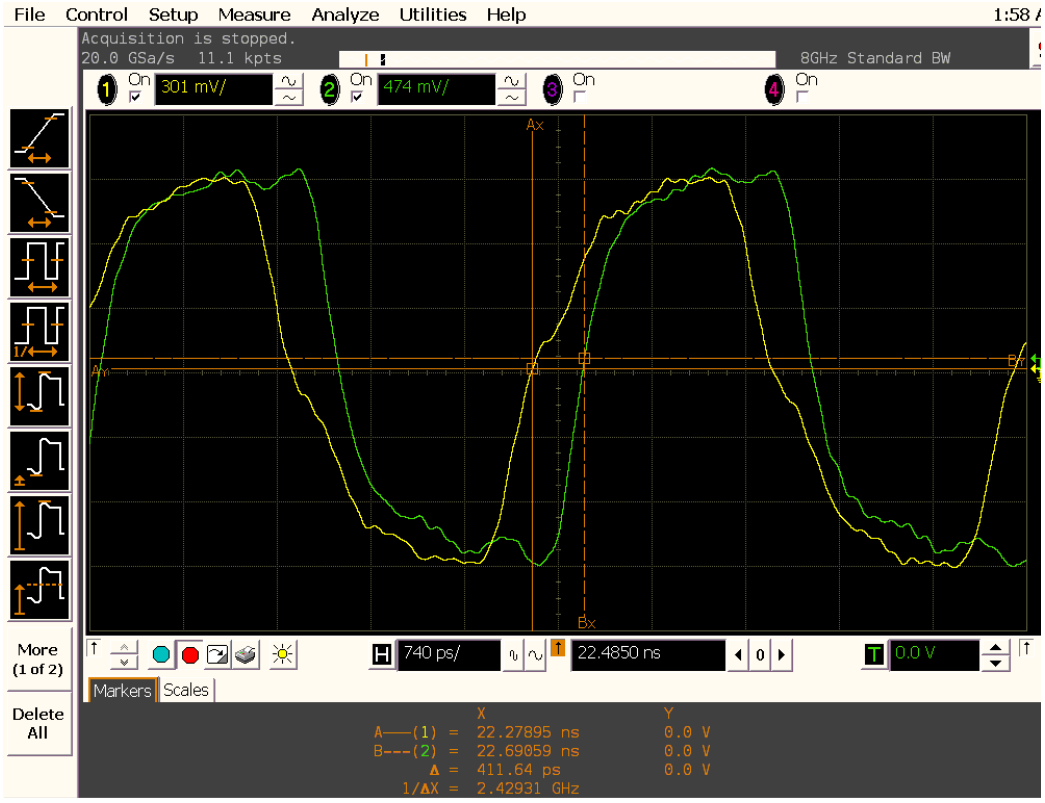

Figure 39 tDQSCK in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 32 DQS Output Access Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-500	+500	-450	+450	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS output access time from CK/$\overline{CK}$	tDQSCK	-400	400	-350	350	ps	40

NOTE 40: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min =- 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min -tERR(6-10per), max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max -tERR(6-10),min = 400 ps. + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ), min(derated) = -900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!).

PASS Condition

The measured time interval between the data strobe access output and the rising edge of the clock should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSCK measurement bit by bit in the Read data burst. Begin at the 1st bit of the Read cycle, from the Read preamble.

11 Continue the measurement until last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 The DQS-Clock timing measurement compares the rising edge (DQS crossing against clock crossing) OR the falling edge (DQS crossing against clock crossing).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

9 Data Strobe Timing (DST) Tests

This section provides the Methods of Implementation (MOIs) for Data Strobe Timing tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Strobe Timing Tests

When performing the Data Strobe Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Data Strobe Timing tests may look similar to the following diagram. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

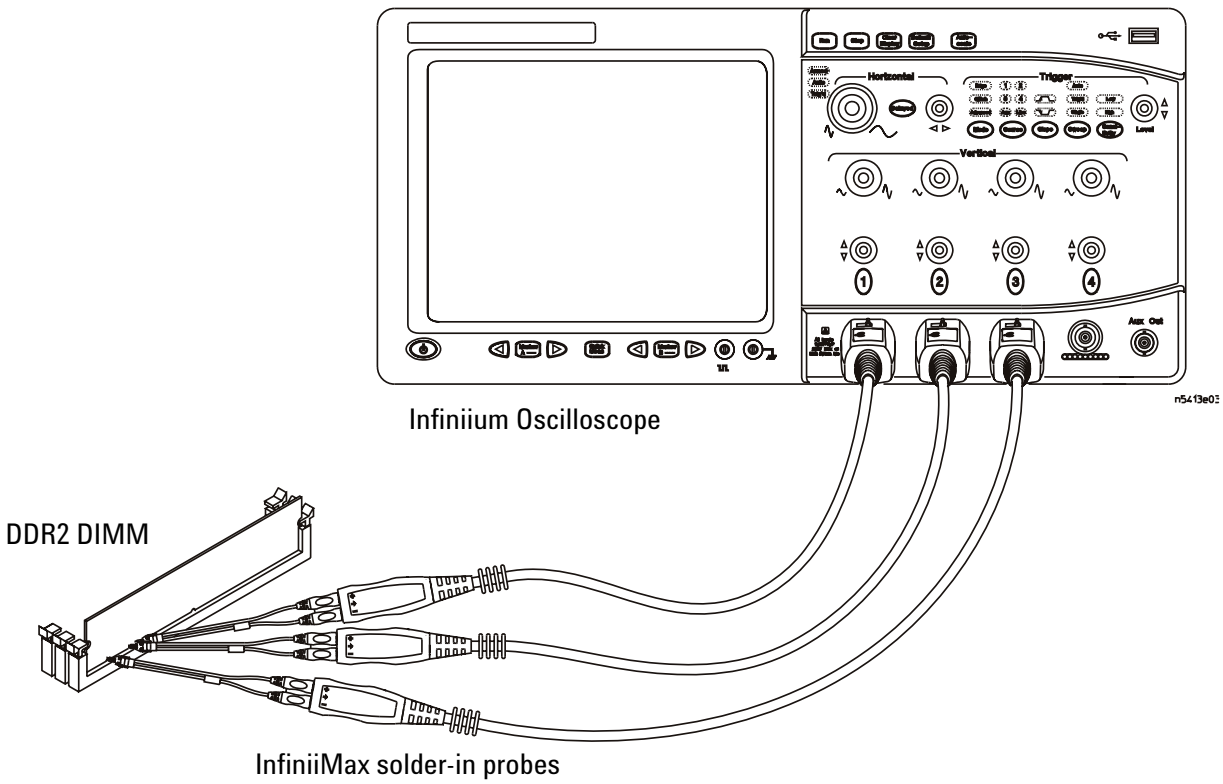

Figure 40 Probing for Data Strobe Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 40 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1 Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Clock Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

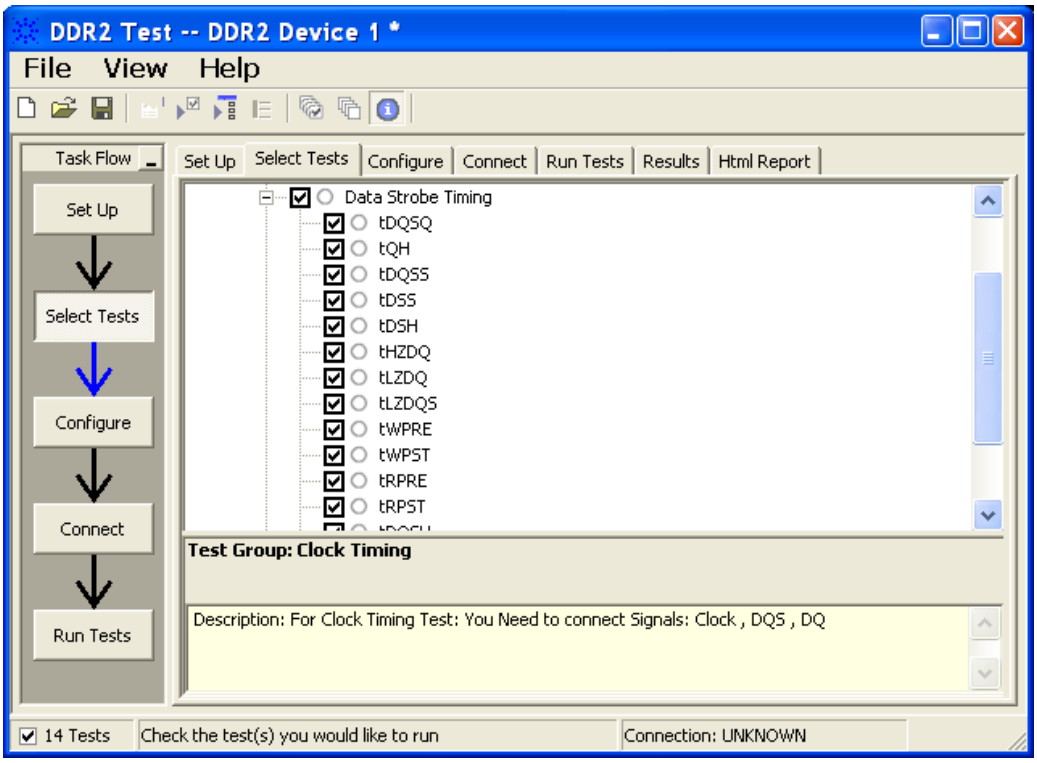

Figure 41 Selecting Data Strobe Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 33), run the tests and view the tests results.

Table 33 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Verify Selected Rank Only?	If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tHZ(DQ), DQ Out High Impedance Time From CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ is no longer driving (from high state OR low state to the high impedance stage), to the clock signal crossing, is within the conformance limits as specified in the *JEDEC Standard JESD79-2C*.

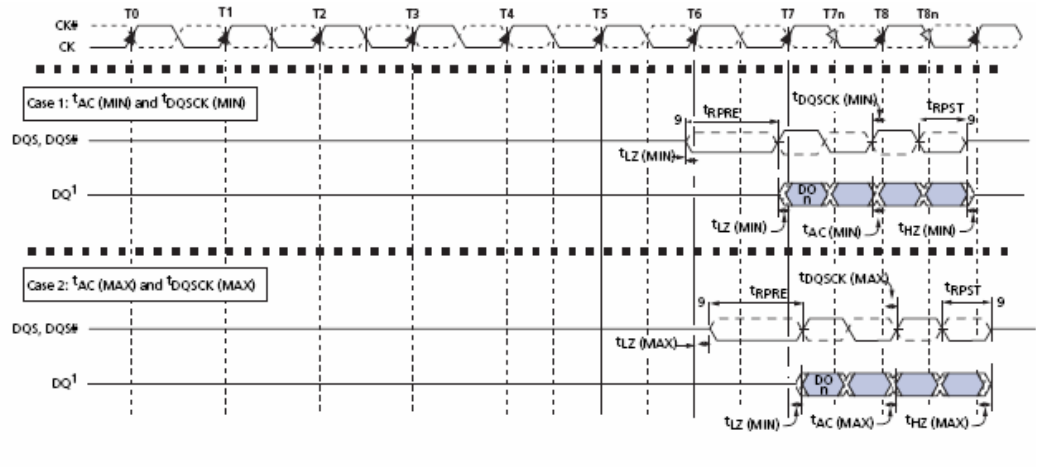

Figure 42 DQ Out High Impedance Time From CK/CK#

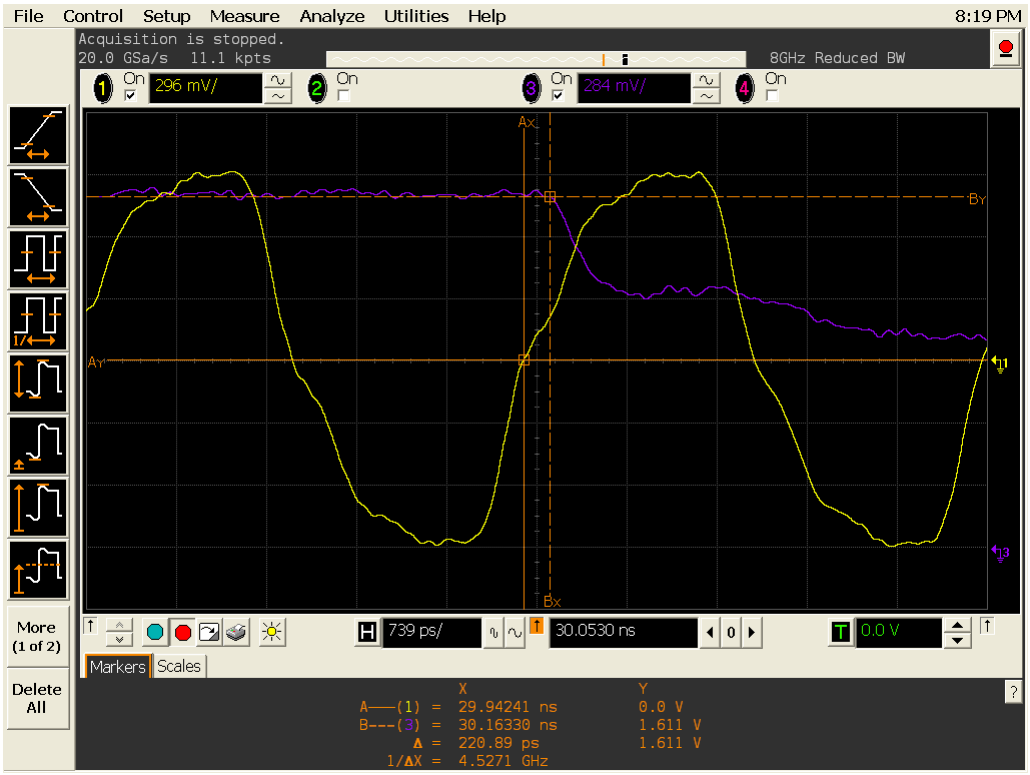

Figure 43 tHZ(DQ) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 34 DQ Out High-Impedance Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	x	tAC max	x	tAC max	ps	18, 40

NOTE 18: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 42 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (U/L/R) DQS each treated as single-ended signal.

NOTE 40: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min =- 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min -tERR(6-10per), max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max -tERR(6-10),min = 400 ps. + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ), min(derated) = -900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!).

PASS Condition

The measured time interval from the point where the DQ starts to transit from high/low state to high impedance state, to the clock signal crossing point should be within the specification limit.

Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function, using Clock as the reference to define the Histogram Window for the DQ signal.

10 The Histogram Window is required to cover the DQ signal from the high/low state to the moment it starts to turn off the driver into tristate.

11 Setup the threshold value and measurement point for the DQ signal based on the histogram result.

12 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQ starts to transit from high/low to the time when it turned off its driver into tristate.

13 Assign marker A for the clock signal crossing point while marker B for the data signal start to turn off its driver.

14 Measure delta of marker A and marker B and this will be the test result.

15 Compare the test result against the compliance test limit.

NOTE Some designs do not have tristate at V_{REF} (for example, 0.9V). This test is not guaranteed when this scenario happens, as there is no significant point of where the driver has been turned-off.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tLZ(DQS), DQS Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts driving (from tristate to high/low state) to the clock signal crossing, is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

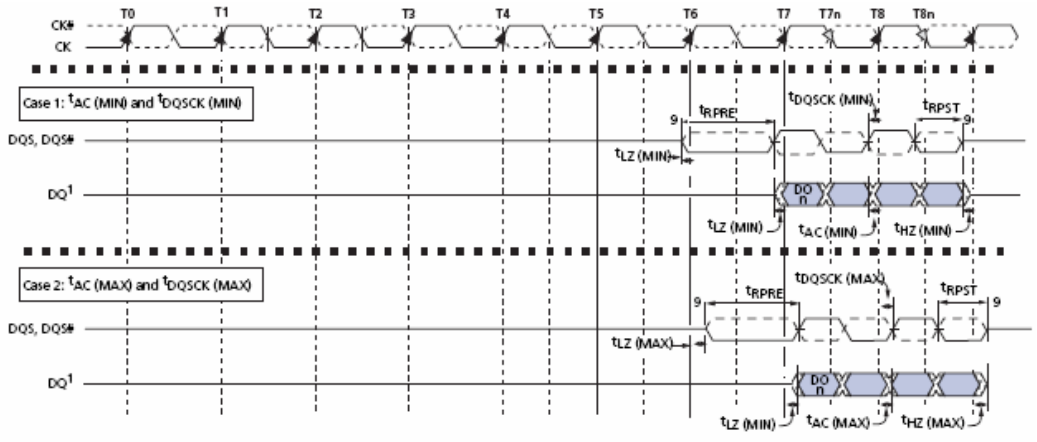

Figure 44 DQS Low-Impedance Time From CK/CK#

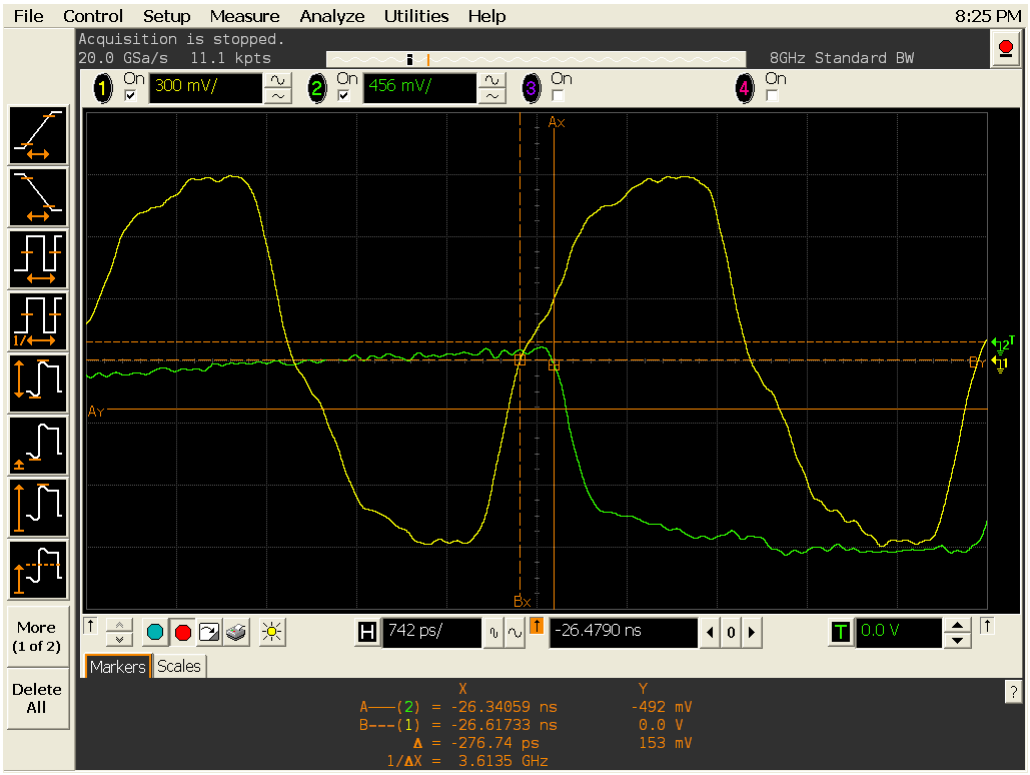

Figure 45 tLZ(DQS) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 35 DQS Low-Impedance Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS/($\overline{\text{DQS}}$) low-impedance time from CK/$\overline{\text{CK}}$	tLZ(DQS)	tAC min	tAC max	tAC min	tAC max	ps	18, 40

NOTE 18: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 44 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (U/L/R) DQS each treated as single-ended signal.

NOTE 40: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min =- 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min -tERR(6-10per), max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max -tERR(6-10),min = 400 ps. + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ), min(derated) = -900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!).

PASS Condition

The measured time interval from the point where the DQS starts to transit from tristate to the moment when it starts to drive high/low (high impedance state to high/low state) to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the "BinaryEdgeNormal" function, using the Clock as the reference to define the Histogram Window for the DQS signal.
10. The Histogram Window is required to cover the DQS signal from tristate to the moment it starts to drive the signal high/low.
11. Setup the threshold value and measurement point for the DQS signal based on the histogram result.
12. Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it start to drive high/low.
13. Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.
14. Measure delta of marker A and marker B and this will be the test result.
15. Compare the test result against the compliance test limit.

Test References

See Table 66 - Timing Parameters by Speed Bin, in the *JEDEC Standard JESD79-2C*.

tLZ(DQ), DQ Low-Impedance Time from CK/CK# - Test Method of Implementation

The purpose of this test is to verify that the time when the DQ starts driving (from high impedance state to high/low state), to the clock signal crossing, is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

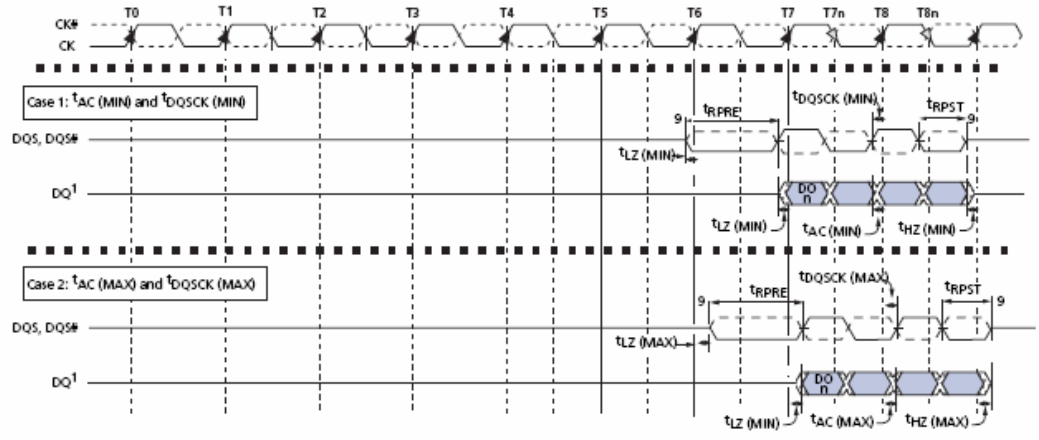

Figure 46 DQ Low-Impedance Time from CK/CK#

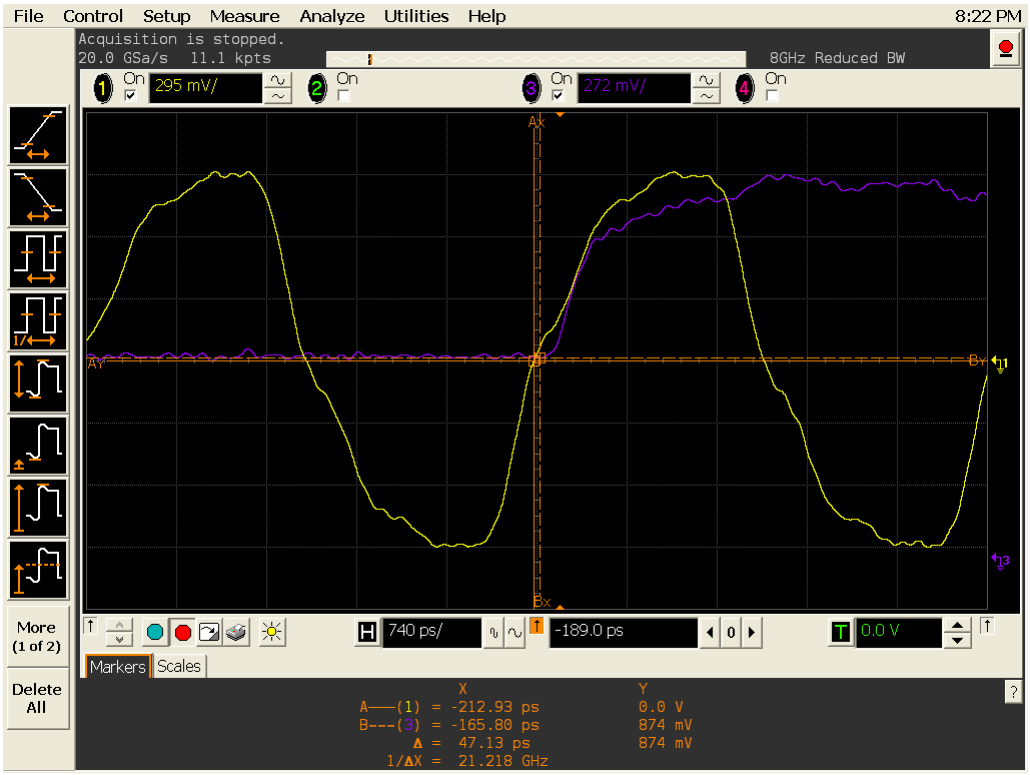

Figure 47 tLZ(DQ) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 36 DQ Low-Impedance Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ low impedance time from CK/CK#	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ low impedance time from CK/CK#	tLZ(DQ)	2 x tAC min	tAC max	2 x tAC min	tAC max	ps	18, 40

NOTE 18: tHZ and tLZ transitions occurs in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begin driving (tLZ). Figure 46 shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. tLZ(DQ) refers to tLZ of the DQ's and tLZ(DQS) refers to tLZ of the (U/L/R) DQS each treated as single-ended signal.

NOTE 40: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per),min =- 272 ps and tERR(6-10per),max = + 293 ps, then tDQSCK,min(derated) = tDQSCK,min -tERR(6-10per), max = - 400 ps - 293 ps = - 693 ps and tDQSCK,max(derated) = tDQSCK,max -tERR(6-10),min = 400 ps. + 272 ps = + 672 ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ), min(derated) = -900 ps - 293 ps = - 1193 ps and tLZ(DQ),max(derated) = 450 ps + 272 ps = + 722 ps. (Caution on the min/max usage!).

PASS Condition

The measured time interval from the point where the DQ starts to transit from high impedance to the moment when it starts to drive high/low (high impedance state to high/low state), to the clock signal crossing point, should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function, using the Clock as the reference to define the Histogram Window for the DQ signal.
10. The Histogram Window is required to cover the DQ signal from the tristate to the moment it starts to drive high/low state.
11. Setup the threshold value and measurement point for the DQ signal based on the histogram result.
12. Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQ starts to transit from tristate to the time when it start to drive the signal high/low.
13. Assign marker A for the clock signal crossing point while marker B for the data signal start to drive.
14. Measure delta of marker A and marker B and this will be the test result.
15. Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDQSQ, DQS-DQ Skew for DQS and Associated DQ Signals - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS rising and falling edge) access time to the associated data (DQ rising and falling) signal is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

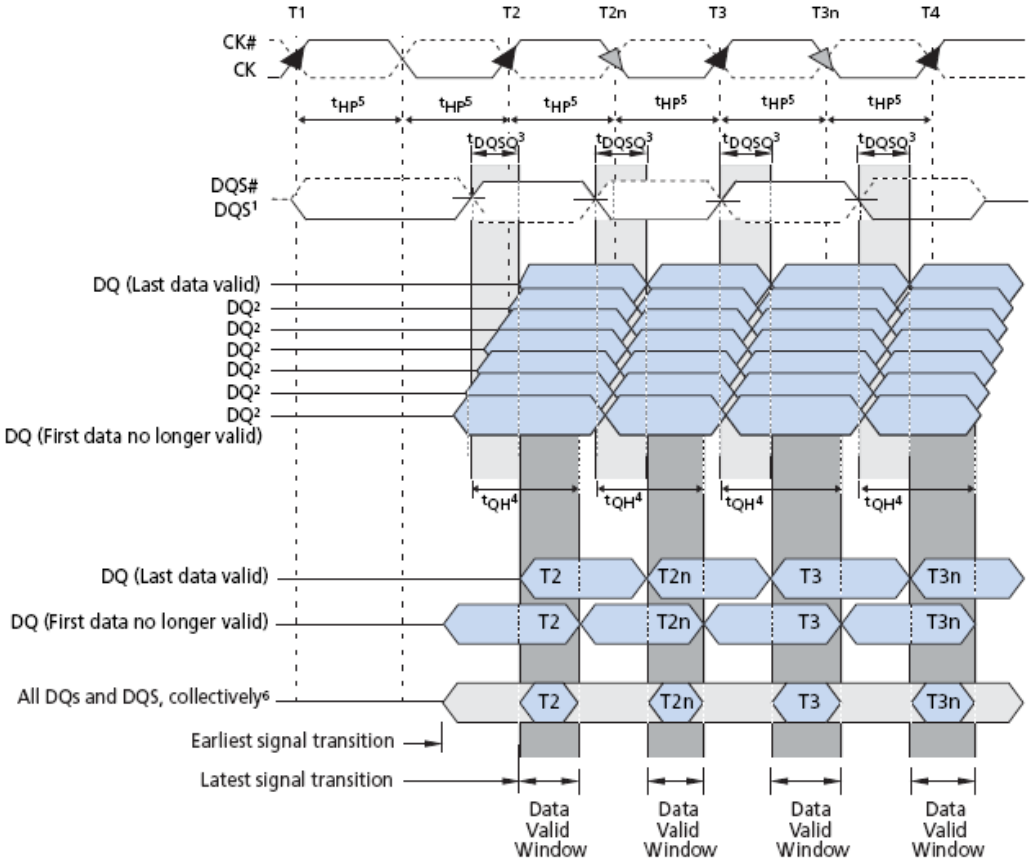

Figure 48 DQS-DQ Skew for DQS and Associated DQ Signals

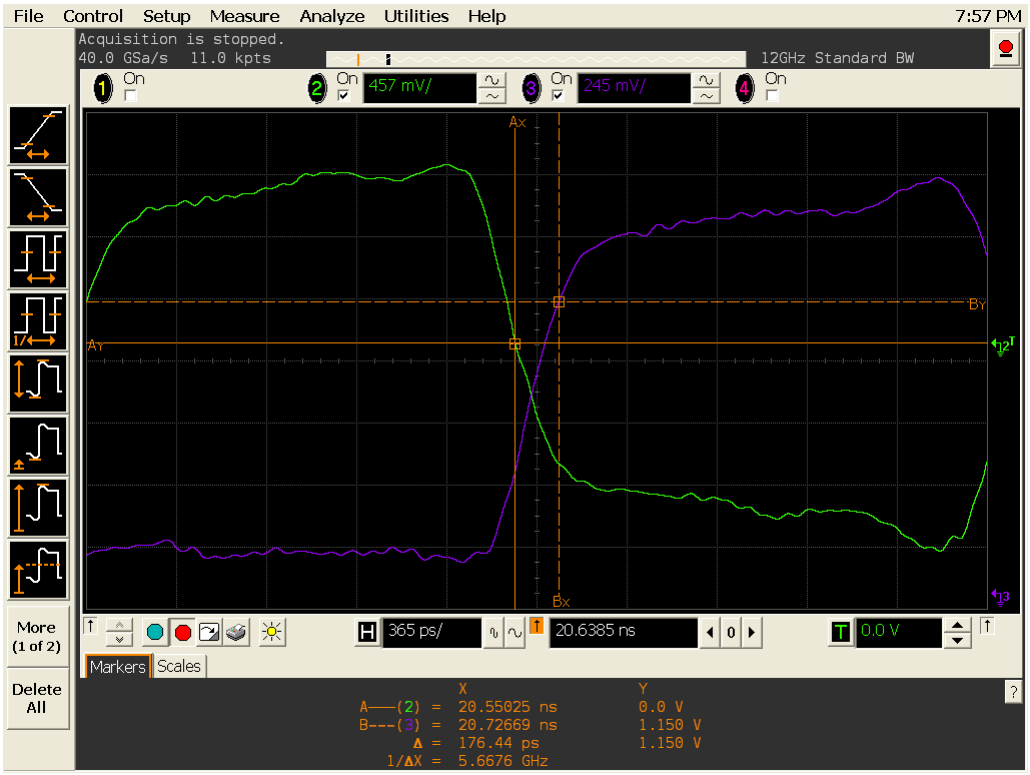

Figure 49 tDQSQ in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 37 DQS-DQ Skew for DQS and Associated DQ Signals Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	x	300	ps	13

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	x	350	-	300	ps	13

NOTE 13: Consists of data pin skew and output pattern effects, and p-channel to n- channel variation of the output drivers as well as output slew rate mismatch between DQS/DQS and associated DQ in any given cycle.

PASS Condition

The measured time interval between the data strobe and the associated data signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Read Cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the DQS and DQ signal. This Edge number will be used for the TEdge measurement, in order to locate the points of interest on specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSQ measurement bit by bit in the Read data burst, beginning from the 1st bit of the Read cycle.

11 Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 DQS-Clock timing measurement compares the rising edge (Vih_ac OR Vil_dc against DQS crossing) OR the falling edge (Vih_ac OR Vil_dc against DQS crossing).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tQH, DQ/DQS Output Hold Time From DQS - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data output hold time (DQS rising and falling edge) from the DQS (rising and falling edge) is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

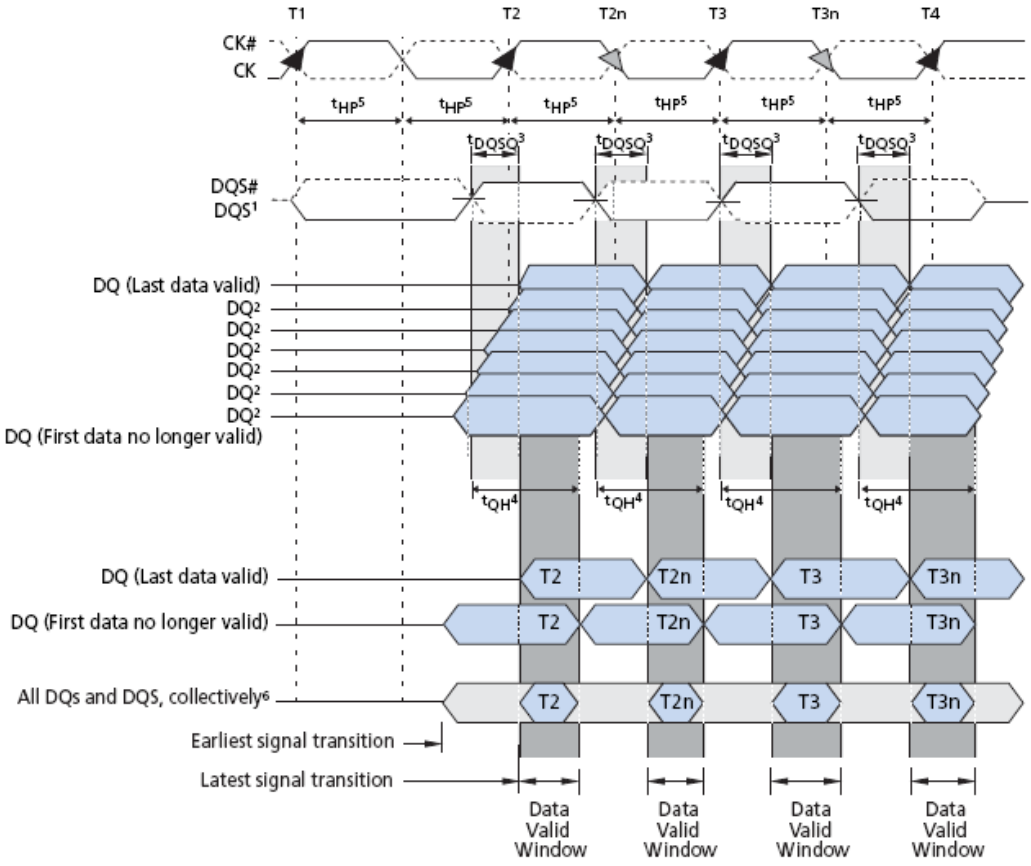

Figure 50 DQ/DQS Output Hold Time From DQS

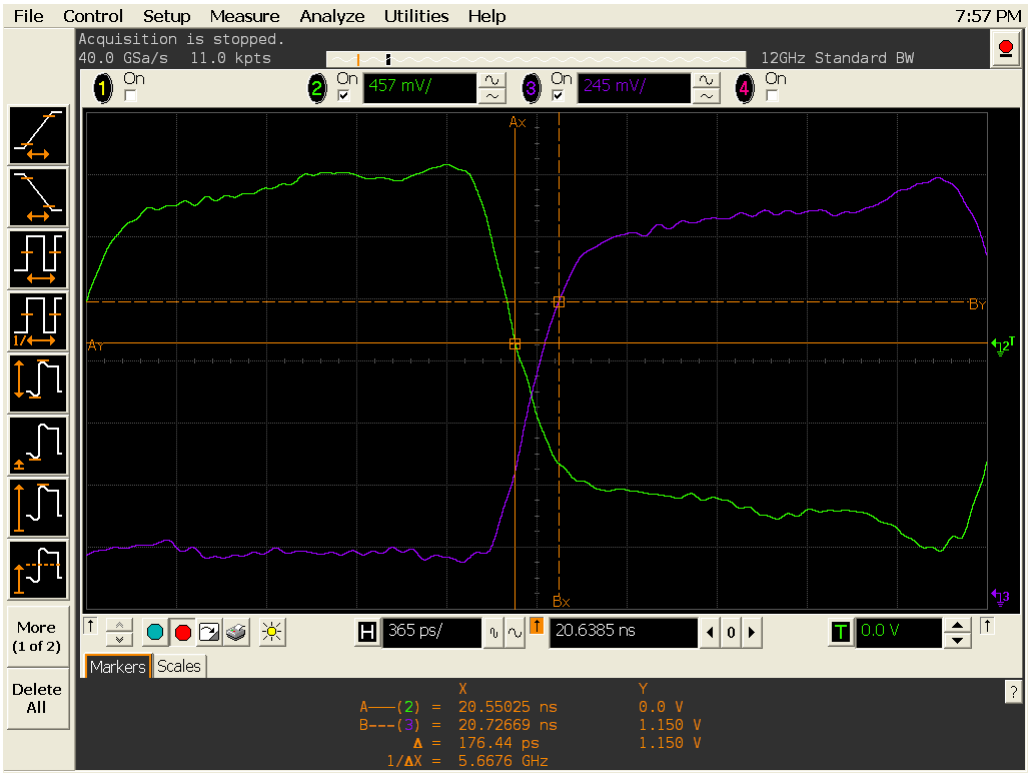

Figure 51 tQH in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 38 DQ/DQS Output Hold Time From DQS Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	tHP-tQHS	x	ps	

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	x	tHP-tQHS	x	ps	39

NOTE 39: tQH= tHP- tQHS, where:

tHP is the minimum of the absolute half period of the actual input clock; and

tQHS is the specification value under the max column.

{The less half- pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

Examples:

1 If the system provides tHP of 1315ps into a DDR2- 667 SDRAM, the DRAM provides tQH of 975ps minimum.

2 If the system provides tHP of 1420ps into a DDR2- 667 SDRAM, the DRAM provides tQH of 1080ps minimum.

PASS Condition

The measured time interval between the data output hold time and the associated data strobe signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the DQS and DQ signal. This Edge number will be used for the TEdge measurement, in order to locate the points of interest on specific signal.

10 After obtaining the Edge number for the respective signal, begin the tQH measurement bit by bit in Read Data Burst, beginning from the 1st bit of the Read cycle.

11 Begin at the 1st bit of the Read cycle, from the Read preamble. Continue the measurement until the last bit (for instance, until a tristate happens, which indicates the end of a data burst for the respective Read cycle).

12 DQS-DQ timing measurement compares the rising edge (DQS crossing against Vil_dc of the DQ signal, for instance, end of valid DQ hold time) OR the falling edge (DQS crossing against Vih_dc of the DQ signal, for instance, end of valid DQ hold time).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the lock signal while marker B for the data signal, for the Worst Case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDQSS, DQS Latching Transition to Associated Clock Edge - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data strobe output (DQS falling edge) access time to the associated clock (crossing point) is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

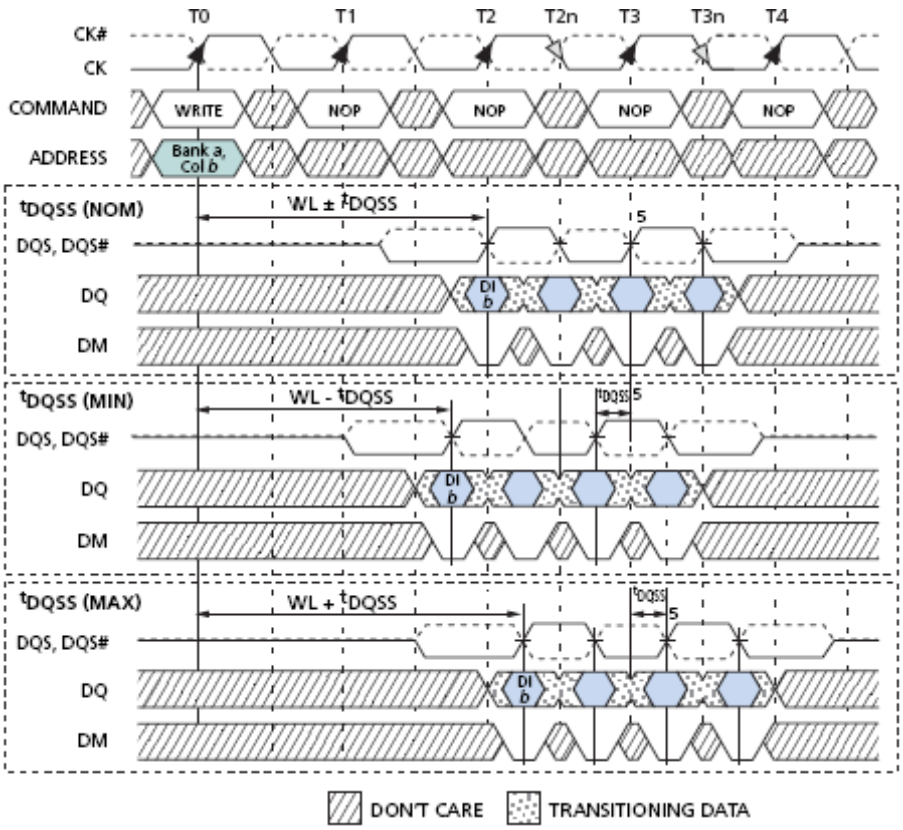

Figure 52 DQS Latching Transition to Associated Clock Edge

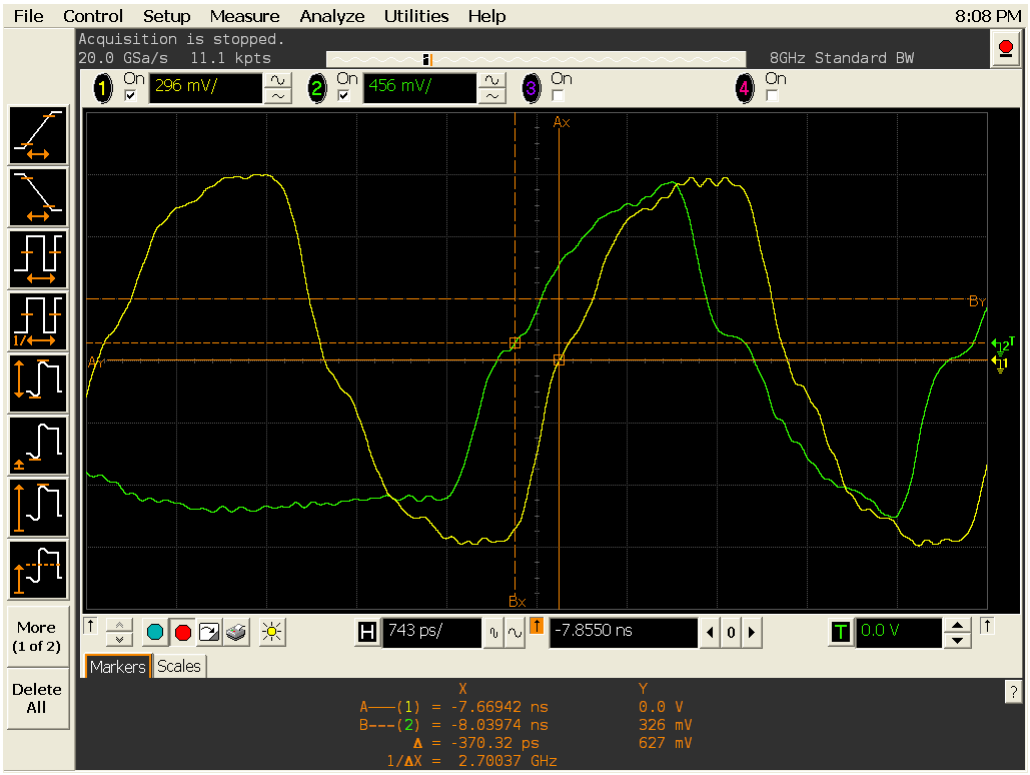

Figure 53 tDQSS in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 39 Timing Parameters by Speed Bin

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK	

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS latching rising transitions to associated clock edges	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)	30

NOTE 30: These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{\text{DQS}}$) crossing to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

PASS Condition

The measured time interval between the rising edge of the data strobe access output and the clock crossing should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{\text{CS}}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{\text{CS}}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of clock rising edge and strobe rising edge. This Edge number will be used for TEdge measurement, in order to locate the points of interest on specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSS measurement bit by bit in the Write data burst, beginning from the 1st bit of the Write cycle. Begin at the 1st bit of the read cycle, from the Write preamble.

11 Continue the measurement until the last bit (for instance, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the rising edge (DQS crossing against clock crossing) OR the falling edge (DQS crossing against Vih_dc of the DQ signal, for instance, end of valid DQ hold time).

13 Within the data burst, measure each bit, for instance the rising edge of the DQS-Clock. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDQSH, DQS Input High Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the high level of the data strobe signal is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

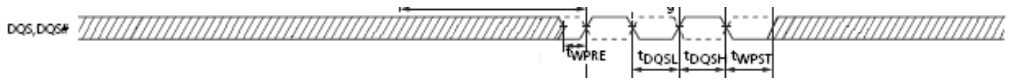

Figure 54 DQS Input High Pulse Width

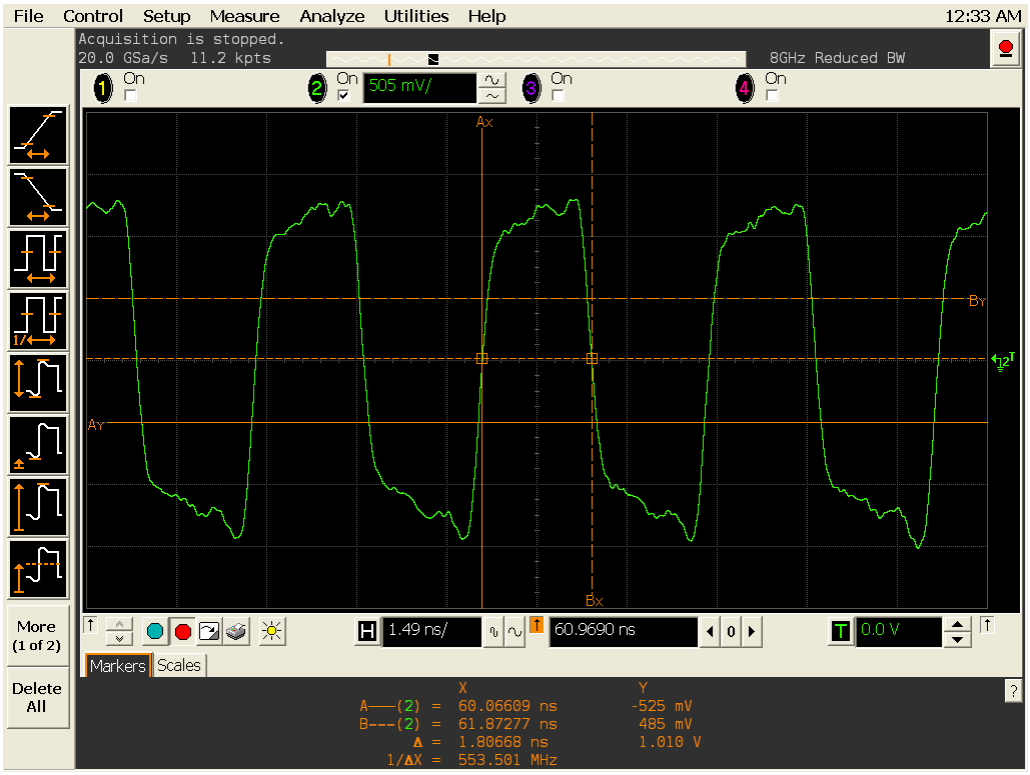

Figure 55 tDQSH in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 40 DQSH Input High Pulse Width Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS input HIGH pulse width	tDQSH	0.35	x	0.35	x	tCK(avg)	

PASS Condition

The measured pwidth of the data strobe signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
4. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
5. If you have selected the $\overline{CS}$ option, skip the next step and go to step 7.
6. Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The for loops, TEdge and Delta Time are used to search the preamble.
7. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

8 After obtaining the Edge number for the respective signal, begin the tDQSH measurement by using the Pwidth function to find any rising edge of the data strobe signal and measure the pwidth for every single bit in the captured data burst.

9 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

10 Measure delta of marker A and marker B and this will be the test result.

11 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDQSL, DQS Input Low Pulse Width - Test Method of Implementation

The purpose of this test is to verify that the width of the low level of the clock signal is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

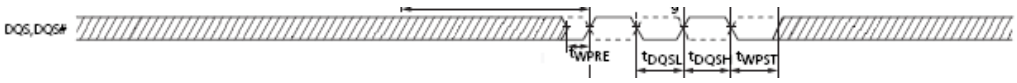

Figure 56 DQS Input Low Pulse Width

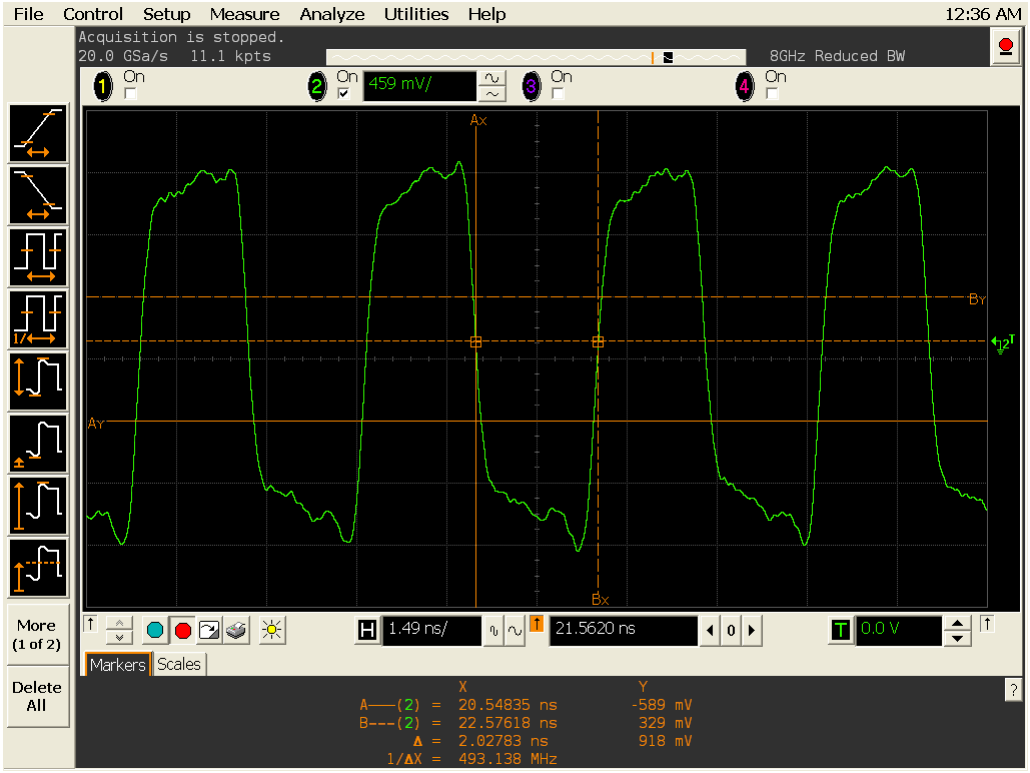

Figure 57 tDQSL in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)

- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 41 DQSL Input Low Pulse Width Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS input LOW pulse width	tDQSL	0.35	x	0.35	x	tCK(avg)	

PASS Condition

The measured nwidth of the clock signal should be within specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The for loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDQSL measurement by using the Nwidth function to find any rising edge of the data strobe signal and measure the nwidth for every single bit in the captured data burst.

11 Assign marker A for the rising edge of the clock signal while marker B for the falling edge of the clock signal.

12 Measure delta of marker A and marker B and this will be the test result.

13 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDSS, DQS Falling Edge to CK Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe (DQS falling edge) output access time to the clock setup time, is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

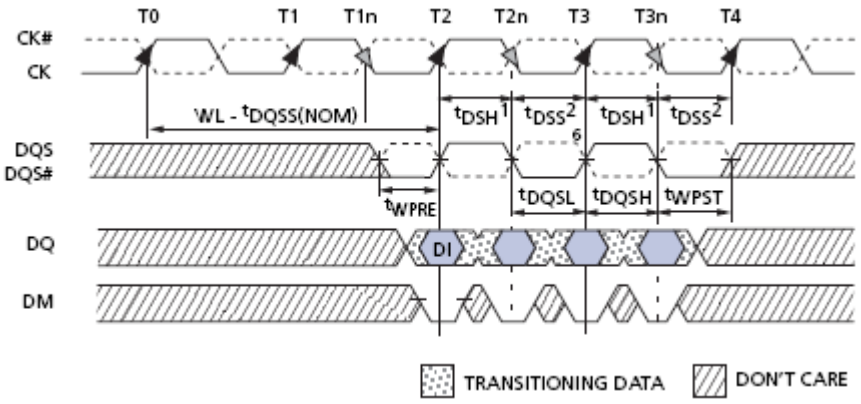

Figure 58 DQS Falling Edge to CK Setup Time

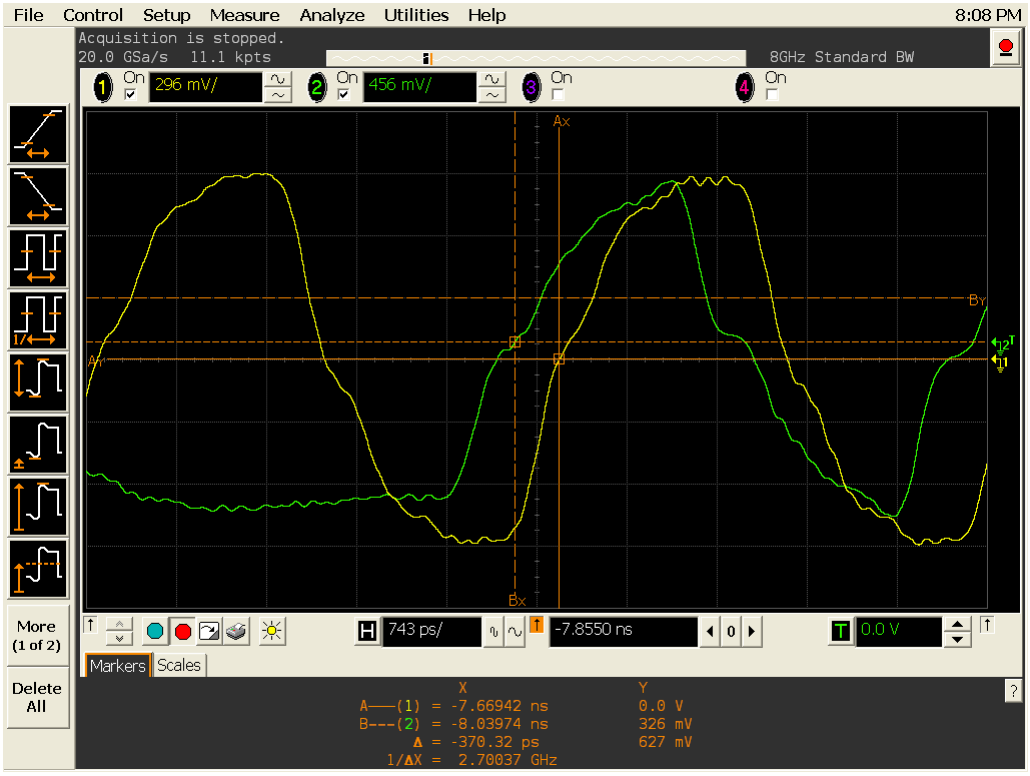

Figure 59 tDSS in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 42 Timing Parameters by Speed Bin

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK(avg)	c

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK(avg)	30

NOTE 30: These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{DQS}$) crossing to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

PASS Condition

The measured time interval between the falling edge of the data strobe access output to the associated clock setup time should be within the specification limit.

Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDSS measurement bit by bit in Write data burst.

11 Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the rising edge (DQS falling against clock crossing).

13 DQ-Clock timing measurement compares the falling edge of the DQS to the clock setup time. The worst case data will be captured each time new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDSH, DQS Falling Edge Hold Time from CK - Test Method of Implementation

The purpose of this test is to verify that the time interval from the falling edge of the data strobe output access time to the hold time of the clock, must be within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

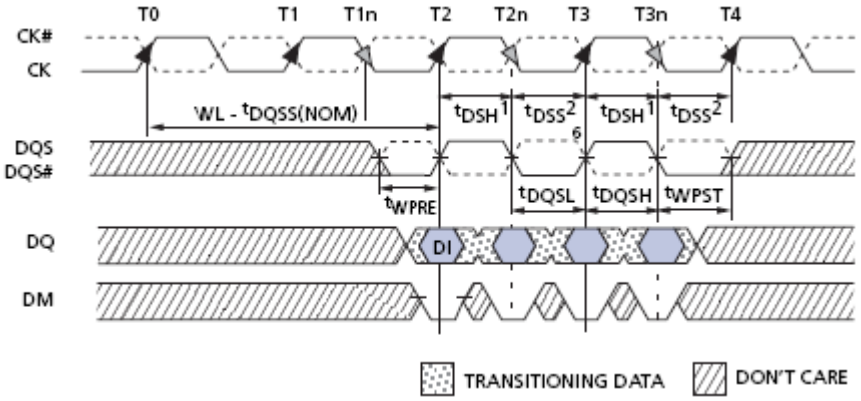

Figure 60 DQS Falling Edge Hold Time

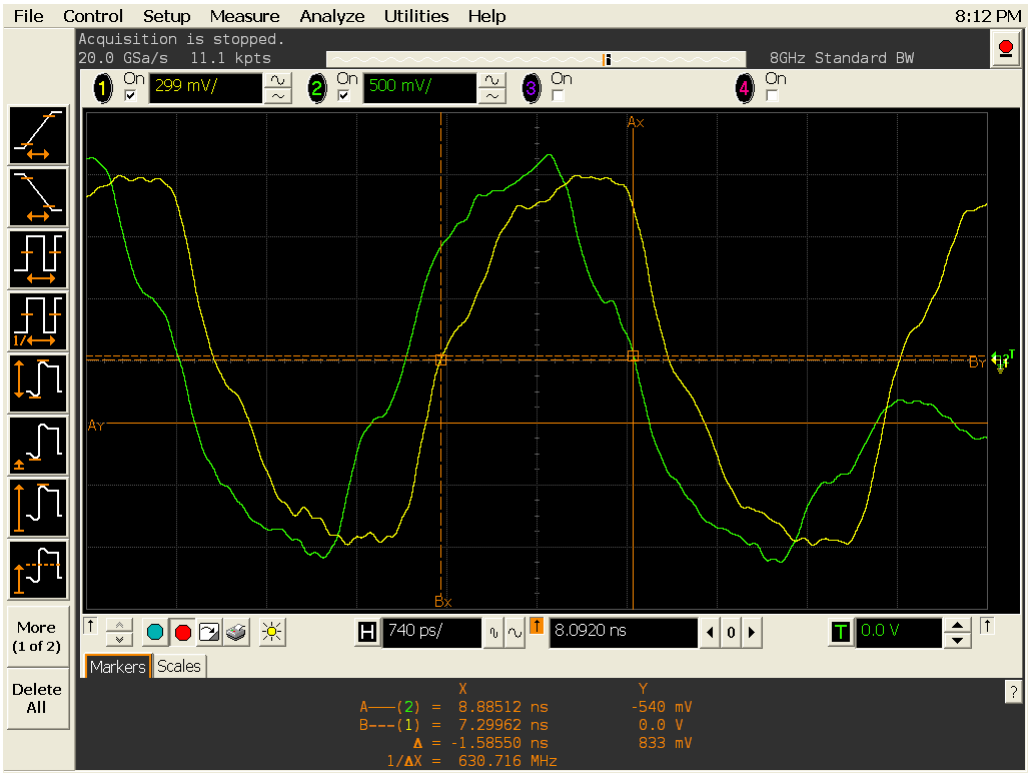

Figure 61 tDSH in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 43 DQS Falling Edge Hold Time Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK	

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
DQS falling edge hold time from CK	tDSH	0.2	x	0.2	x	tCK(avg)	30

NOTE 30: These parameters are measured from a data strobe signal ((L/U/R)DQS/$\overline{\text{DQS}}$) crossing to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

PASS Condition

The measured time interval between the falling edge of the data strobe hold time from the associated clock crossing edge should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{\text{CS}}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{\text{CS}}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{\text{CS}}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDSH measurement bit by bit in Write data burst.

11 Begin at the 1st bit of the Write cycle, from the Write preamble. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-Clock timing measurement compares the falling edge of the DQS crossing hold time from the respective clock crossing edge.

13 Within the data burst, each bit, for instance, the falling edge of DQS-Clock will be measured. The worst case data will be captured each time a new value is measured.

14 Once all the bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tWPST, Write Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high impedance) from the last DQS signal crossing (last bit of the write data burst) for the Write cycle, is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

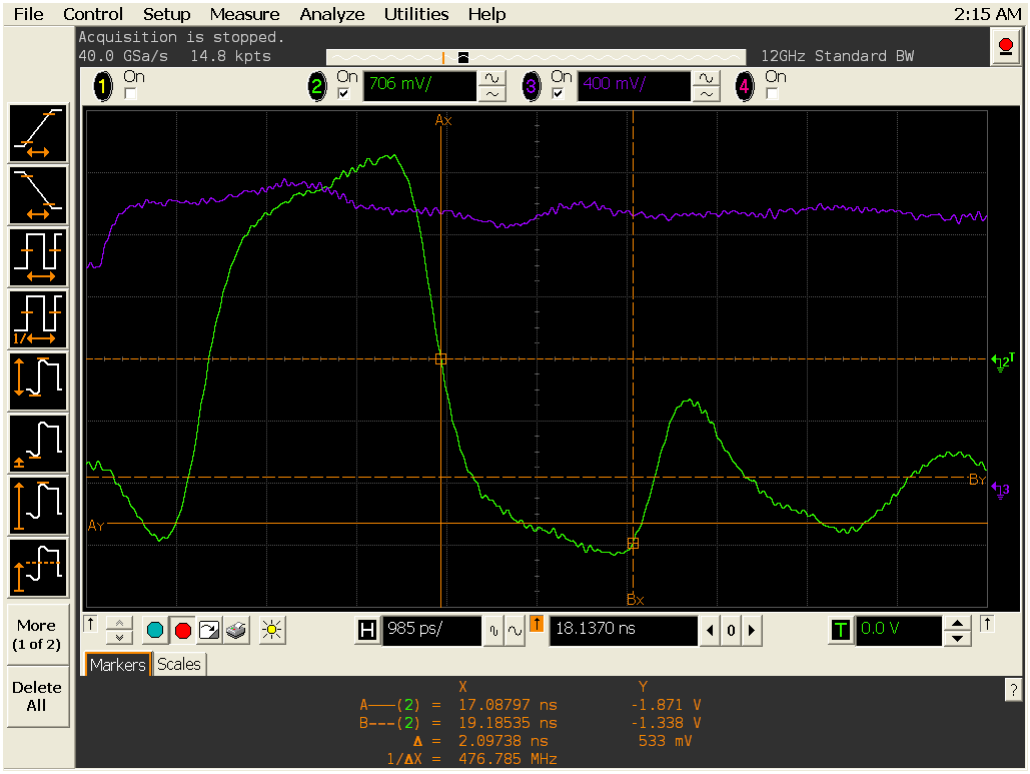

Figure 62 tWPST in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 44 Write Postamble Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Postamble	tWPST	0.4	0.6	0.4	0.6	tCK	10

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Postamble	tWPST	0.4	0.6	0.4	0.6	tCK(avg)	10

NOTE 10: The maximum limit for this parameter is not device limit. The device will operate with greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

PASS Condition

The measured time interval between the last DQS signal crossing point and the point where the DQS starts to transit from high/low state to high impedance should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS postamble towards the right from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the postamble.

9 Once the postamble is located, call the “BinarySearchNormal” function to locate the last DQS crossing point or reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS postamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it starts to turn off the driver low (for instance, end of burst or postamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off driver.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tWPRE, Write Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS starts to drive low (preamble behavior) to the first DQS signal crossing for the Write cycle, is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

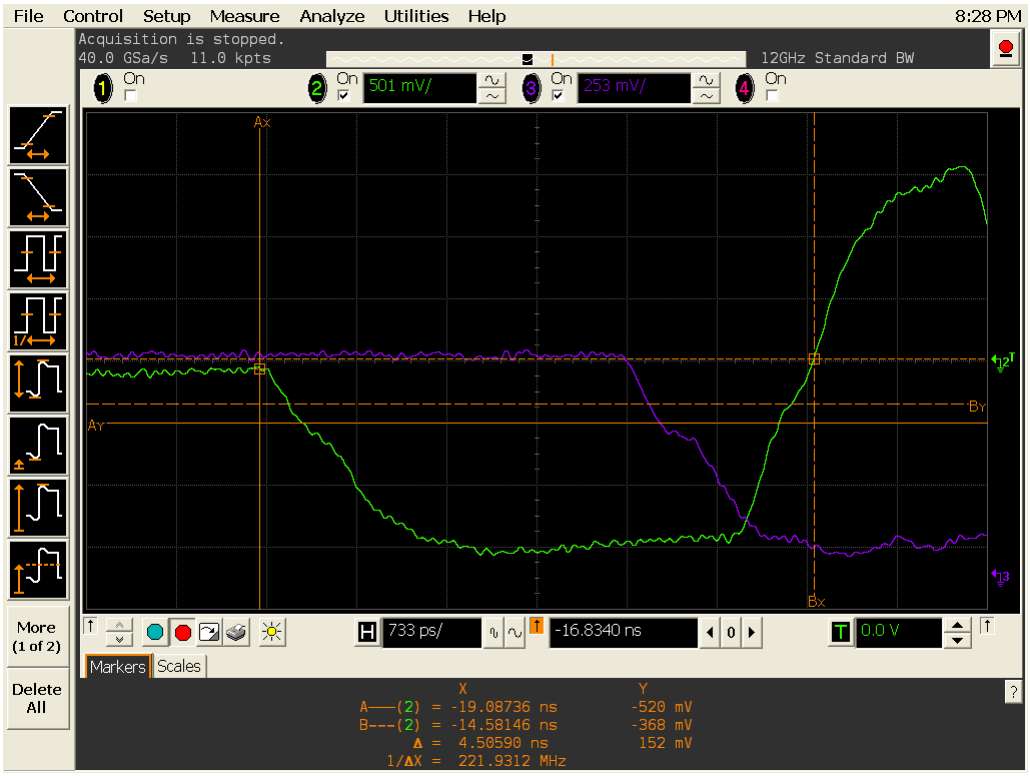

Figure 63 tWPRE in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 45 Write Preamble Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Preamble	tWPRE	0.35	x	0.35	x	tCK	

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
WRITE Preamble	tWPRE	0.35	x	0.35	x	tCK(avg)	

PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Write cycle, should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinarySearchNormal” function to locate the first DQS crossing point or the reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS preamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it starts to drive low (for instance, beginning of preamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tRPRE, Read Preamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS start driving low (*preamble behavior) to the first DQS signal crossing for the Read cycle must be within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

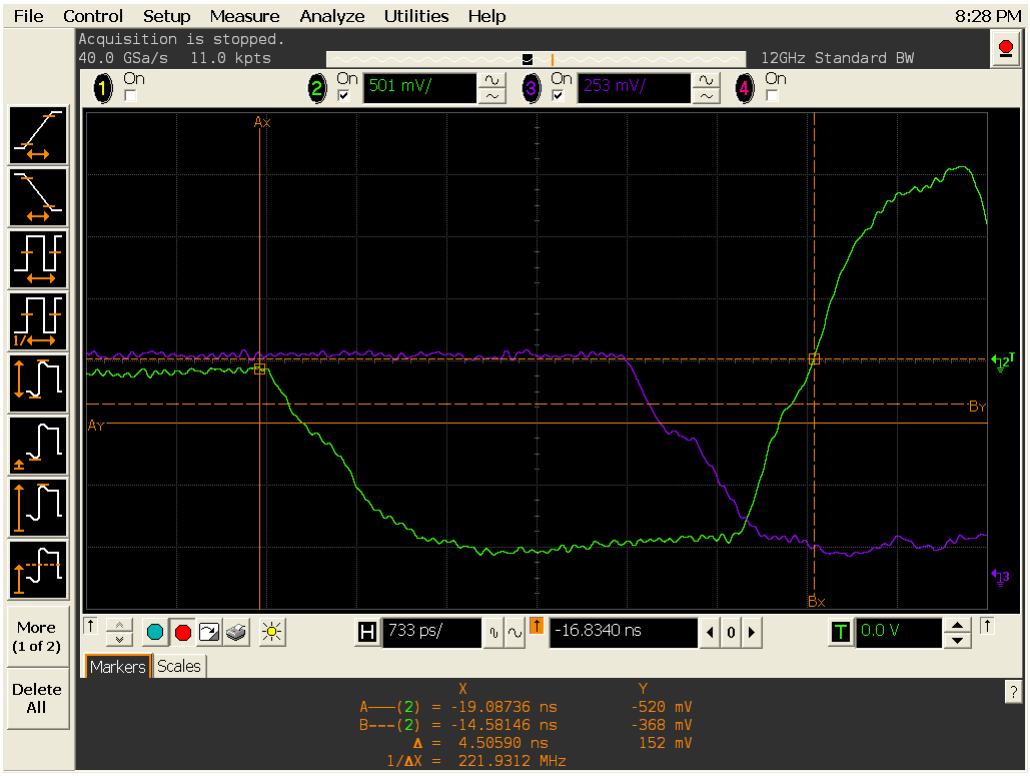

Figure 64 tRPRE in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 46 Read Preamble Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
READ Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	19

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
READ Preamble	tRPRE	0.9	1.1	0.9	1.1	tCK(avg)	19, 41

NOTE 19: tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). The actual voltage measurement points are not critical as long as the calculation is consistent.

NOTE 41: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2- 667 SDRAM has tJIT(per), min = - 72ps and tJIT(per), max = +93ps, then tRPRE, min(derated) = tRPRE, min + tJIT(per), min = 0.9 x tCK(avg) - 72ps = +2178ps and tRPRE, max(derated) = tRPRE, max + tJIT(per), max = 1.1 x tCK(avg) + 93ps = +2843ps. (Caution on the min/max usage!).

PASS Condition

The measured time interval of the point where the DQS starts to transit from tristate (high impedance state to low state) to the DQS signal crossing point for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the “BinarySearchNormal” function to locate the first DQS crossing point or the reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS preamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all the points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from tristate to the time when it start to drive low (for instance, beginning of preamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to drive low.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tRPST, Read Postamble - Test Method of Implementation

The purpose of this test is to verify that the time when the DQS is no longer driving (from high/low state to high-impedance) to the last DQS signal crossing (last bit of the data burst) for the Read cycle is within the conformance limit as specified in the *JEDEC Standard JESD79-2C*.

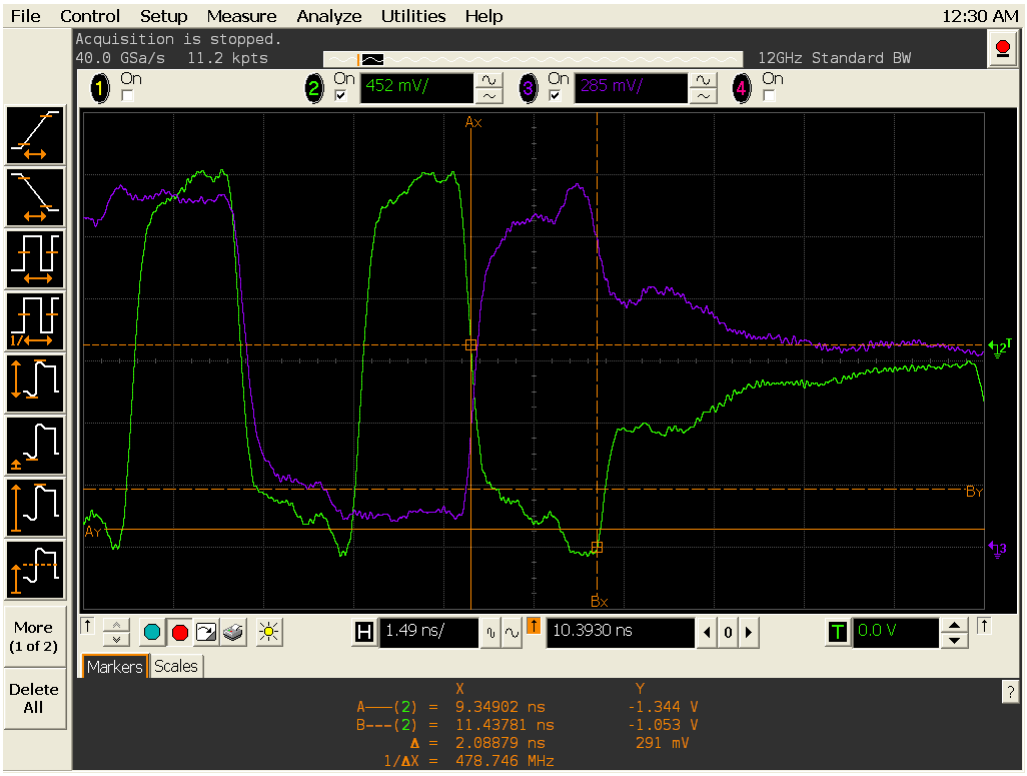

Figure 65 tRPST in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Data Strobe Signal (DQS as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Strobe Signal (DQS as Pin Under Test Signal)
- Data Signal (DQ as Supporting Signal)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 47 Read Postamble Test

Parameter	Symbol	DDR2-800		DDR2-1066		Units	Specific Notes
		Min	Max	Min	Max		
READ Postamble	tRPST	0.4	0.6	0.4	0.6	tCK)	19

Parameter	Symbol	DDR2-1333		DDR2-1600		Units	Specific Notes
		Min	Max	Min	Max		
READ Postamble	tRPST	0.4	0.6	0.4	0.6	tCK(avg)	19, 42

NOTE 19: tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). The actual voltage measurement points are not critical as long as the calculation is consistent.

NOTE 42: When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2- 667 SDRAM has tJIT(duty), min = - 72ps and tJIT(duty), max = +93ps, then tRPST, min(derated) = tRPST, min + tJIT(duty), min = 0.4 x tCK(avg) - 72ps = +928ps and tRPST, max(derated) = tRPST, max + tJIT(duty), max = 0.6 x tCK(avg) + 93ps = +1592ps. (CAution on the min/max usage!)

PASS Condition

The measured time interval between the last DQS signal crossing point to the point where the DQS starts to transit from high/low level to high impedance for the Read cycle should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope setting. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS postamble towards the right from the point where the Read cycle was previously captured. The For loops, TEdge and Delta Time are used to search the postamble.

9 Once the postamble is located, call the “BinarySearchNormal” function to locate the last DQS crossing point or reference point.

10 Define the histogram window in order to obtain the Min and Max voltage for the DQS postamble signal and it will be used for the threshold setup for the trigonometry calculation later.

11 Once all points are obtained, proceed with the trigonometry calculation to find the point where the DQS starts to transit from high/low to the time when it starts to turn off the driver low (for instance, end of burst, postamble).

12 Assign marker A for the DQS signal crossing point while marker B for the data strobe signal start to turn off the driver.

13 Measure delta of marker A and marker B and this will be the test result.

14 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

10
Data Mask Timing (DMT) Tests

This section provides the Methods of Implementation (MOIs) for Data Mask Timing tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Data Mask Timing Tests

When performing the Data Mask Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Data Mask Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

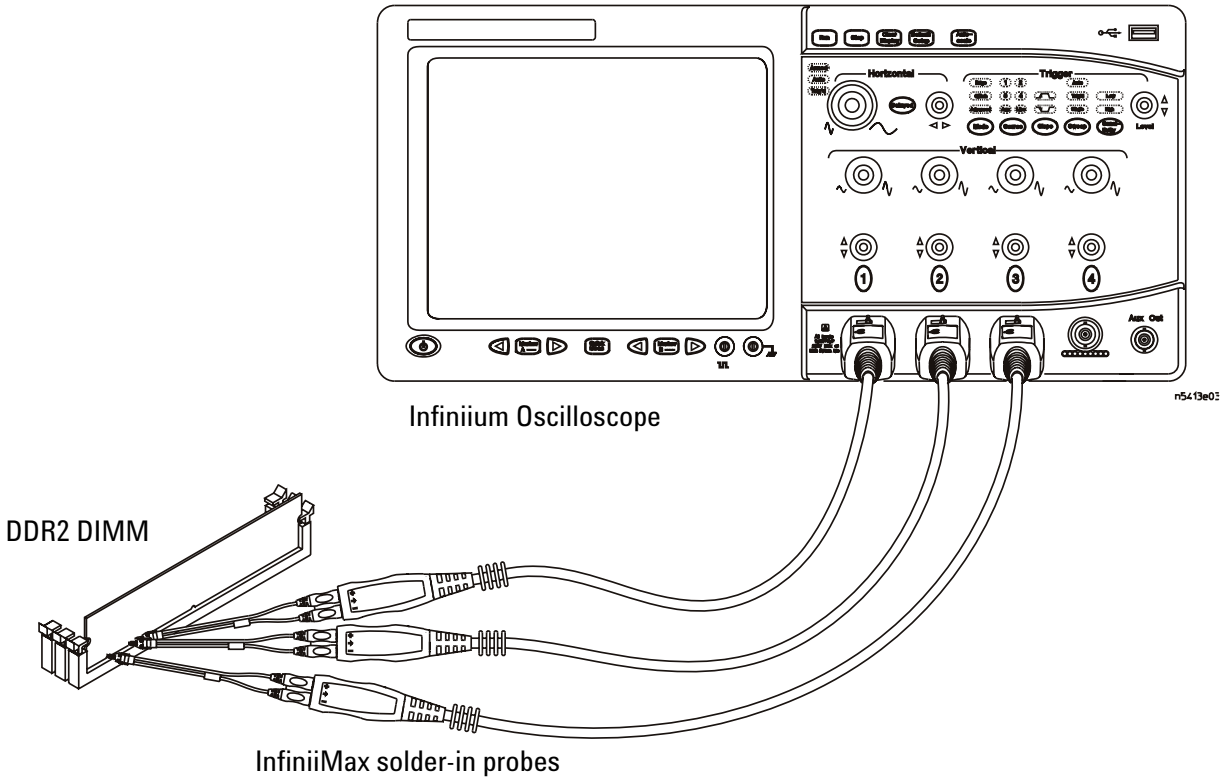

Figure 66 Probing for Data Mask Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 66 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1. Start the automated test application as described in “Starting the DDR2 Compliance Test Application" on page 27.
2. Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.
3. Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.
4. Connect the oscilloscope probes to any channels of the oscilloscope.
5. In the DDR2 Test application, click the Set Up tab.
6. Select the Speed Grade options. For Data Mask Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.
7. Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.
8. Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

Figure 67 Selecting Data Mask Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 48), run the tests and view the tests results.

Table 48 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Verify Selected Rank Only?	If you choose Yes, you require an additional channel for the Chip Select (CS). Measurement will only be done on the selected rank based on the Chip Select signal connected to the oscilloscope.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tDS(base), Differential DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling Edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-2C*.

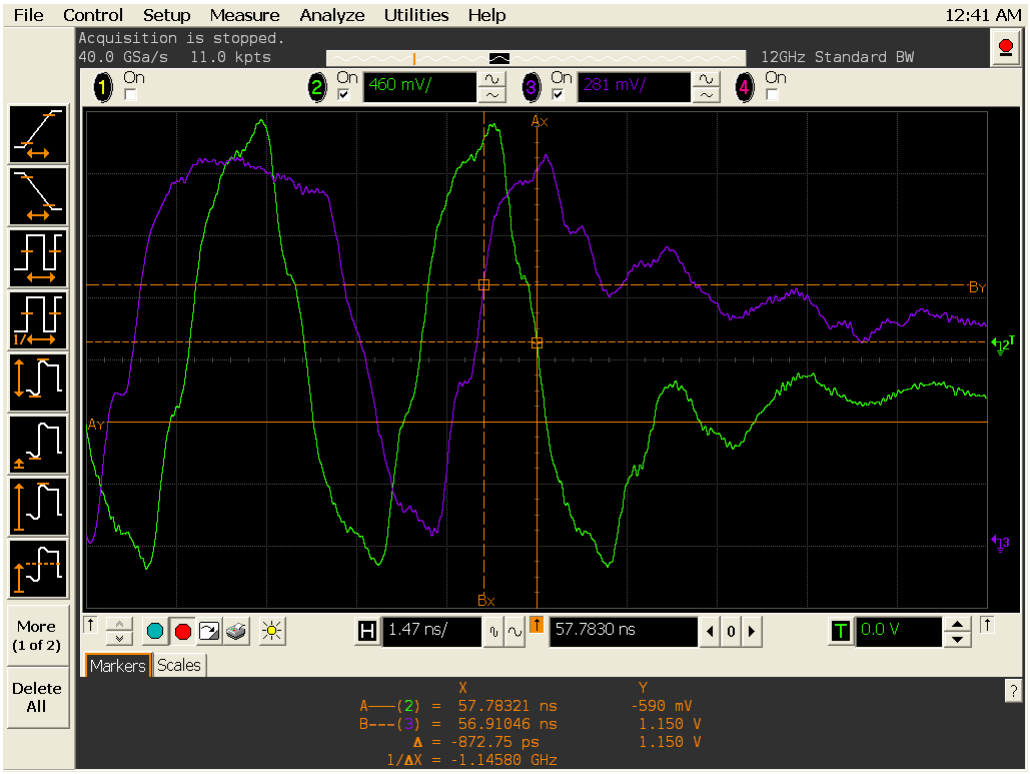

Figure 68 tDS(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires additional channel)

Test Definition Notes from the Specification

Table 49 DQ and DM Input Setup Time (Differential) Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (differential strobe)	tDS(base)	150	x	100	x	ps	6,7,8,20,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time	tDS(base)	100	x	50	x	ps	6,7,8,20,28,31

NOTE 6: Timings are specified with DQs, DM and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

NOTE 7: Timings are specified with CK/CK# differential slew rate of 2.0V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

NOTE 8: Data setup and hold time derating. See Table 43 - DDR2 - 400/533 tDS/tDH Derating With Differential Data Strobe and Table 44 - DDR2 - 667/800 tDS/tDH Derating With Differential Data Strobe.

NOTE 20: Input waveform timing tDS with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

NOTE 28: If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

NOTE 31: These parameters are measured from a data signal (L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/DQS#) crossing.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the rise/fall DQS crossing and Vih_ac/Vil_ac DQ for later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.
10. After obtaining the Edge number for the respective signal, begin the tDS(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.
11. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).
12. The DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vih_ac against associated DQS crossing) OR the falling edge (DQ falling, for instance Vil_ac against associated DQS crossing).
13. Within the data burst, measure each bit, for instance rising and falling edge of DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDH(base), Differential DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-2C*.

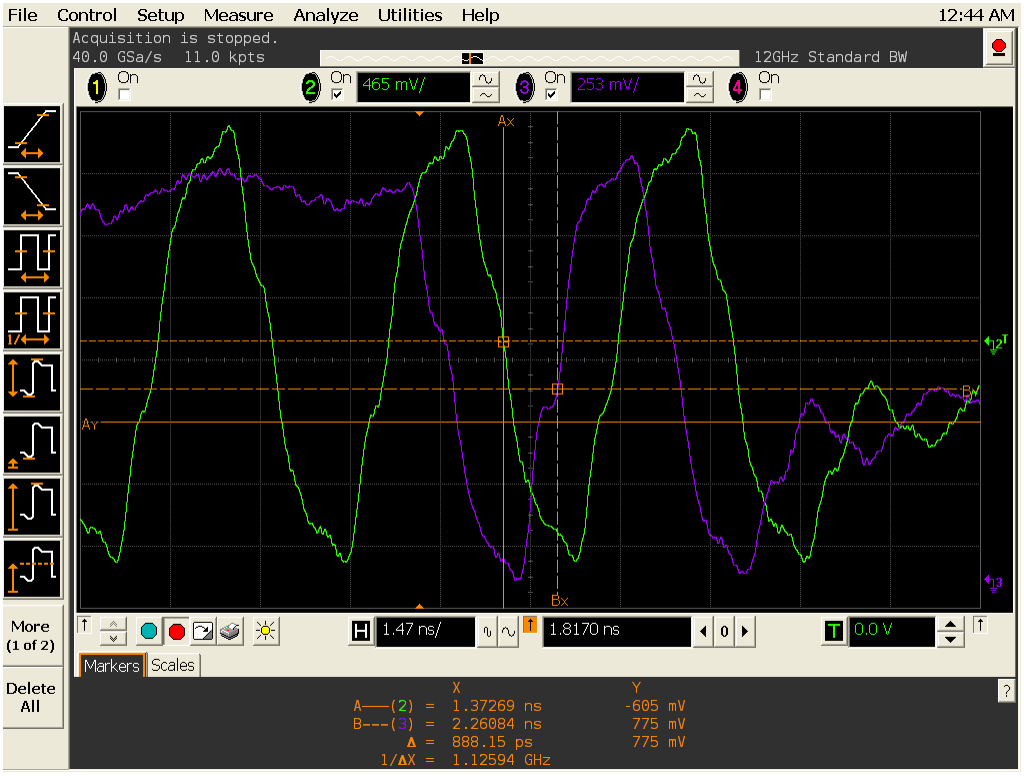

Figure 69 tDH(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use differential connection (DQS+ and DQS-)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 50 DQ and DM Input Hold Time (Differential) Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (differential strobe)	tDH(base)	275	x	225	x	ps	6,7,8,21,28

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time	tDH(base)	175	x	125	x	ps	6,7,8,21,28,31

NOTE 6: Timings are specified with DQs, DM and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

NOTE 7: Timings are specified with CK/CK# differential slew rate of 2.0V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

NOTE 8: Data setup and hold time derating. See Table 43 - DDR2 - 400/533 tDS/tDH Derating With Differential Data Strobe and Table 44 - DDR2 - 667/800 tDS/tDH Derating With Differential Data Strobe.

NOTE 21: Input waveform timing tDH with differential data strobe enabled MR[bit10]=0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH(dc)}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL(dc)}$ level for a rising signal applied to the device under test. DQS, DQS# signals must be monotonic between Vil(dc)max and Vih(dc)min.

NOTE 28: If tDS or tDH is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

NOTE 31: These parameters are measured from a data signal (L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS/DQS#) crossing.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) hold time to the respective DQS crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.
5. Chip Select ($\overline{CS}$) option is only applicable if the user has selected “Yes” for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.
6. Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.
7. If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.
8. Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.
9. Once the preamble is located, call the “BinaryEdgeNormal” function to obtain the Edge number of the rise/fall DQS crossing and the Vih_dc/Vil_dc DQ for the later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.
10. After obtaining the Edge number for the respective signal, begin the tDH(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.
11. Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).
12. The DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vil_dc against associated DQS crossing) OR the falling edge (DQ falling, for instance Vih_dc against associated DQS crossing).
13. Within the data burst, measure each bit, for instance rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tDS1(base), Single-Ended DQ and DM Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) setup time to the associated DQS edge is within the conformance limits as specified in the *JEDEC Standard JESD79-2C*.

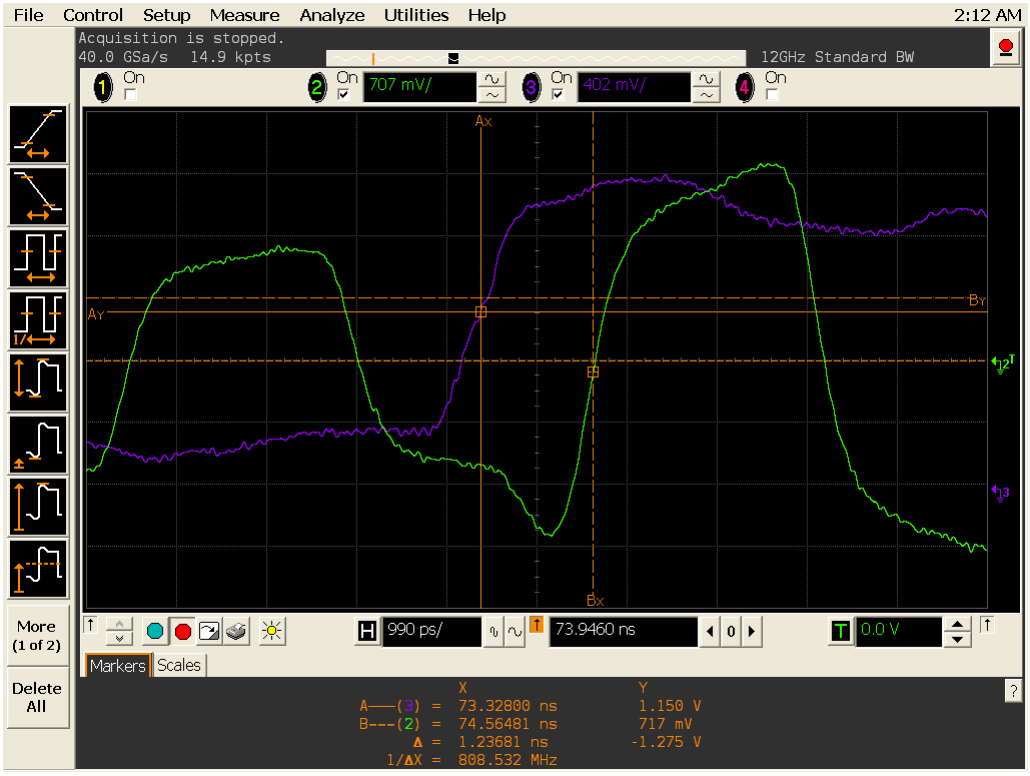

Figure 70 tDS1(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use single-ended (DQS+ with ground)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 51 DQ and DM Input Setup Time (Single-Ended) Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input setup time (single-ended strobe)	tDS1(base)	25	x	-25	x	ps	6,7,8,25

NOTE 6: Timings are specified with DQs, DM and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

NOTE 7: Timings are specified with CK/CK# differential slew rate of 2.0V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

NOTE 8: Data setup and hold time derating. See Table 43 - DDR2 - 400/533 tDS/tDH Derating With Differential Data Strobe and Table 44 - DDR2 - 667/800 tDS/tDH Derating With Differential Data Strobe.

NOTE 25: Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between $V_{il(dc)max}$ and $V_{ih(dc)min}$.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS edge should be within the specification limit.

Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number of the rise/fall Vil_dc/Vih_dc DQS and Vih_ac/Vil_ac DQ for later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDS1(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.

11 Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a Data Burst for the respective Write cycle).

12 DQS-DQ timing measurement compares the rising edge (DQ rising, for instance Vih_ac against associated DQS rising(Vil_dc) OR falling(Vih_dc).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) in the *JEDEC Standard JESD79-2C*.

tDH1(base), Single-Ended DQ and DM Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the data or data mask (DQ/DM rising/falling edge) hold time to the associated DQS edge is within the conformance limits as specified in the *JEDEC Standard JESD79-2C*.

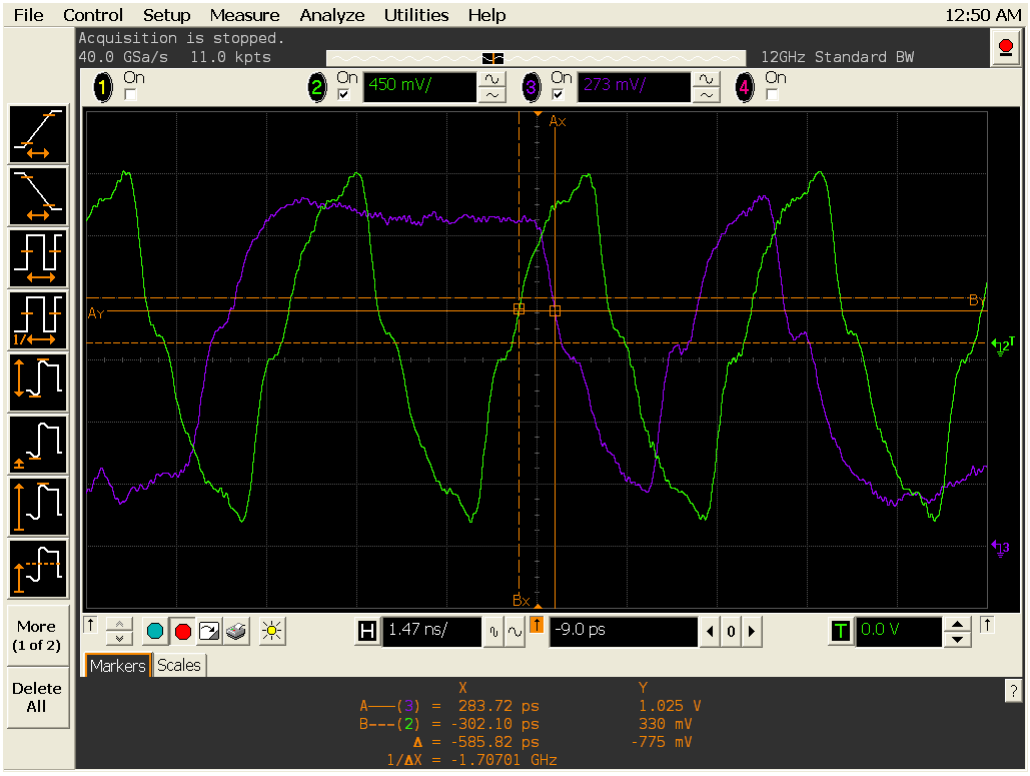

Figure 71 tDH1(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)
  - Use single-ended (DQS+ with ground)
- Clock Signal (CK as Reference Signal)

Optional signal required to separate the signals for the different Ranks:

- Chip Select Signal ($\overline{CS}$ as additional signal, which requires an additional channel)

Test Definition Notes from the Specification

Table 52 DQ and DM Input Hold Time (Single-Ended) Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
DQ and DM input hold time (single-ended strobe)	tDH1(base)	25	x	-25	x	ps	6,7,8,26

NOTE 6: Timings are specified with DQs, DM and DQS's (DQS/RDQS in single ended mode) input slew rate of 1.0V/ns. See Specific Notes on derating for other slew rate values.

NOTE 7: Timings are specified with CK/CK# differential slew rate of 2.0V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

NOTE 8: Data setup and hold time derating. See Table 43 - DDR2 - 400/533 tDS/tDH Derating With Differential Data Strobe and Table 44 - DDR2 - 667/800 tDS/tDH Derating With Differential Data Strobe.

NOTE 26: Input waveform timing with single-ended data strobe enabled MR[bit10]=1, is referenced from the input signal crossing at the $V_{IH(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(ac)}$ at the start of its transition for a rising signal, and from the input signal crossing at the $V_{IL(dc)}$ level to the single-ended data strobe crossing $V_{IH/L(dc)}$ at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between $V_{il(dc)max}$ and $V_{ih(dc)min}$.

PASS Condition

The measured time interval between the data or data mask (DQ/DM) setup time to the respective DQS edge should be within the specification limit.

Measurement Algorithm

1 Obtain the parameters and settings from the Configuration page.

2 Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.

3 Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.

4 Perform signal skew checking on the DQ-DQS to ensure that it can be triggered during the Read/Write separation later.

5 Chip Select ($\overline{CS}$) option is only applicable if the user has selected "Yes" for the Verify Selected Rank Only option in the Configuration page. It uses the $\overline{CS}$-DQS for signal separation. Else, by default, the DQS-DQ is used for signal separation.

6 Use the InfiniiScan feature with the Setup time and Hold time to find and capture the Read cycle.

7 If you have selected the $\overline{CS}$ option, skip the next step and go to step 9.

8 Search for the DQS preamble towards the left from the point where the Write cycle was previously captured. The For loops, TEdge and Delta Time are used to search the preamble.

9 Once the preamble is located, call the "BinaryEdgeNormal" function to obtain the Edge number of the rise/fall Vih_ac/Vil_ac DQS and Vih_dc/Vil_dc DQ for later TEdge measurement use. This Edge number will be used to locate the point of interest on the specific signal.

10 After obtaining the Edge number for the respective signal, begin the tDH1(base) measurement bit by bit in the Write data burst. Begin at the 1st bit of the Write cycle, from the Write preamble.

11 Continue the measurement until the last bit (for example, until a tristate happens, which indicates the end of a data burst for the respective Write cycle).

12 DQS-DQ timing measurement compares the DQ edge (DQ rising, for instance Vil_dc/DQ falling, for instance Vih_dc against associated DQS rising(Vih_ac) OR falling (Vil_ac).

13 Within the data burst, measure each bit, for instance the rising and falling edge of the DQS-DQ. Capture the worst case data each time a new value is measured.

14 Once all bits are validated, assign marker A for the clock signal while marker B for the data signal, for the worst case bit.

15 Measure delta of marker A and marker B and this will be the test result.

16 Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) in the *JEDEC Standard JESD79-2C*.

11 Command and Address Timing (CAT) Tests

This section provides the Methods of Implementation (MOIs) for Command and Address Timing tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

NOTE Both XYZ# and $\overline{\text{XYZ}}$ are referring to compliment. Thus, CK# is the same as $\overline{\text{CK}}$.

Probing for Command and Address Timing Tests

When performing the Command and Address Timing tests, the DDR2 Compliance Test Application will prompt you to make the proper connections. The connection for Command and Address Timing tests may look similar to the following diagrams. Refer to the Connection tab in DDR2 Electrical Performance Compliance Test application for the exact number of probe connections. Typically, you need minimum three probe connections to run the tests.

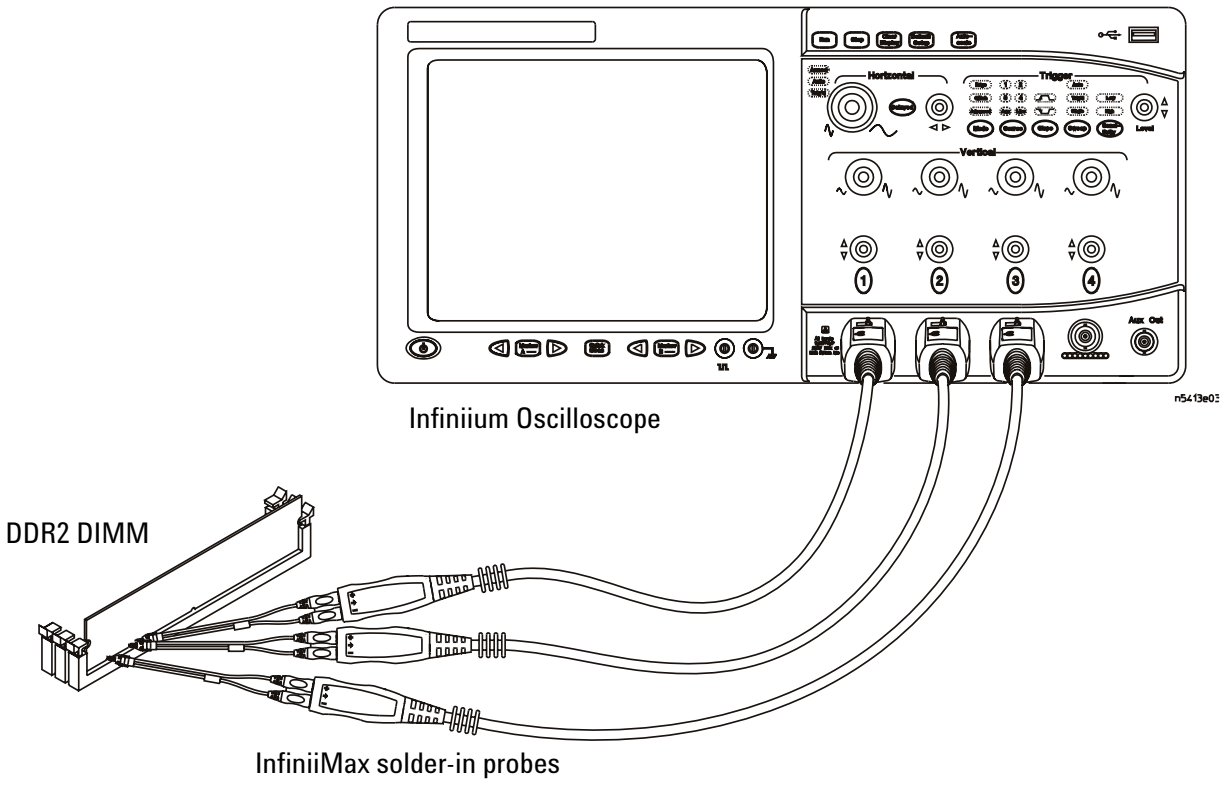

Figure 72 Probing for Command and Address Timing Tests with Three Probes

You can use any of the oscilloscope channels as Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 72 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer system where the DDR2 Device Under Test (DUT) is attached. This software will perform test on all the unused RAM on the system by producing repetitive burst of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.

4 Connect the oscilloscope probes to any channels of the oscilloscope.

5 In the DDR2 Test application, click the Set Up tab.

6 Select the Speed Grade options. For Command and Address Timing Tests, you can select any speed grade within the selection: DDR2-400, DDR2-533, DDR2-667, DDR2-800.

7 Type in or select the Device Identifier as well as User Description from the drop-down list. Enter your comments in the Comments text box.

8 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

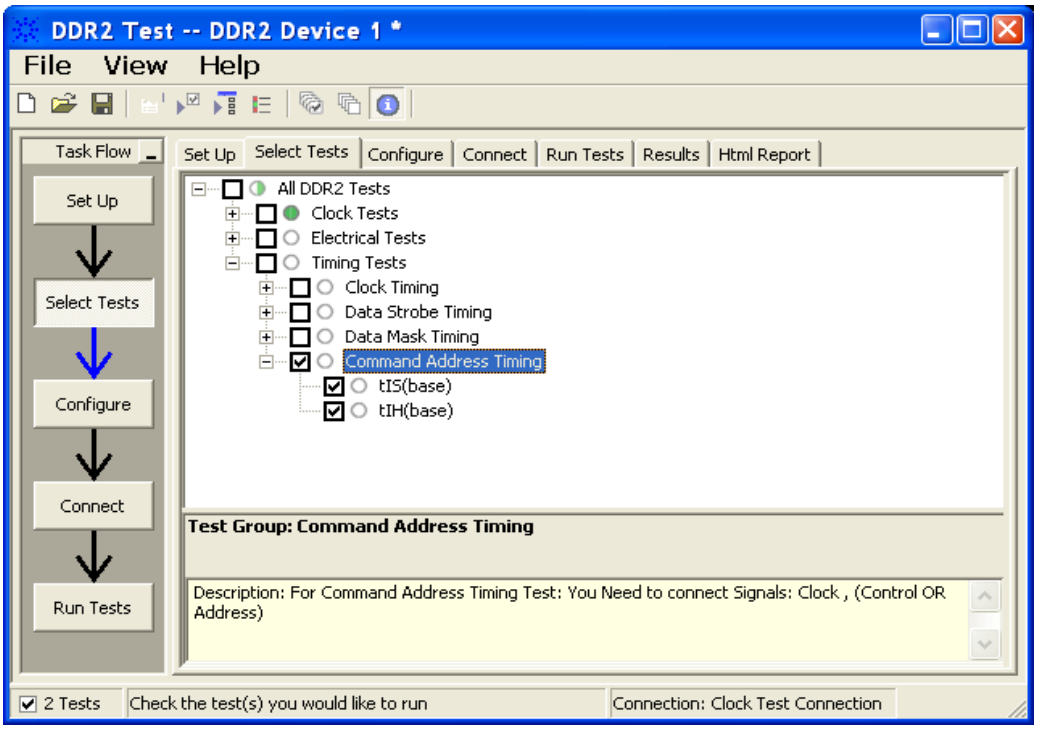

Figure 73 Selecting Command and Address Timing Tests

9 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 53), run the tests and view the tests results.

Table 53 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Timing Tests	
Total Bit Display	Allows you to select the number of data bits to be displayed at the end of the test. Selecting more bits gives a better view of the entire burst of signals.
Total Measurement Required	To perform the total number of measurement based on your selection.
Channel (1,2,3)	Signal connected to the specific channel.
Pin Under Test, PUT	Signal used for testing.

tIS(base) - Address and Control Input Setup Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) setup time to the associated clock crossing edge is within the conformance limits of the $V_{ID(ac)}$ as specified in the *JEDEC Standard JESD79-2C*.

Figure 74 tIS(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 54 Address and Control Input Setup Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	350	x	250	x	ps	5,7,9,22

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input setup time	tIS(base)	200	x	175	x	ps	5,7,9,22,29

NOTE 5: Timing are specified with command/address input slew rate of 1.0 V/ns. See Specific Notes on derating for other slew rate values.

NOTE 7: Timing are specified with CK/CK# differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

NOTE 9: See Table 46 - Derating Values for DDR2-400, DDR2-533 and Table 46 - Derating Values for DDR2-667, DDR2-800 in the *JEDEC Standard JESD79-2C*.

NOTE 22: Input waveform timing is referenced from the input signal crossing at the $V_{IH(ac)}$ level for a rising signal and $V_{IL(ac)}$ for a falling signal applied to the device under test.

NOTE 29: These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

PASS Condition

The measured time interval between the address/control setup time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the CK-DQS.
5. tIS measurement will compare the rising edge (address/control rising e.g. Vih_ac against associated clock crossing) OR falling edge (address/control falling e.g. Vil_ac against associated clock crossing).
6. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

tIH(base) - Address and Control Input Hold Time - Test Method of Implementation

The purpose of this test is to verify that the time interval from the address or control (rising or falling edge) hold time to the associated clock crossing edge is within the conformance limits as specified in the *JEDEC Standard JESD79-2C*.

Figure 75 tIH(base) in Infiniium oscilloscope

Signals of Interest

Based on the test definition (Read cycle only):

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Signals required to perform the test on the oscilloscope:

- Address and Control Signal (as Pin Under Test Signal)
- Clock Signal (CK as Reference Signal)

Test Definition Notes from the Specification

Table 55 Address and Control Input Setup Time Test

Parameter	Symbol	DDR2-400		DDR2-533		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	475	x	375	x	ps	5,7,9,23

Parameter	Symbol	DDR2-667		DDR2-800		Units	Specific Notes
		Min	Max	Min	Max		
Address and control input hold time	tIH(base)	275	x	250	x	ps	5,7,9,23,29

NOTE 5: Timing are specified with command/address input slew rate of 1.0 V/ns. See Specific Notes on derating for other slew rate values.

NOTE 7: Timing are specified with CK/CK# differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1 V/ns in single ended mode. See Specific Notes on derating for other slew rate values.

NOTE 9: See Table 46 - Derating Values for DDR2-400, DDR2-533 and Table 46 - Derating Values for DDR2-667, DDR2-800 in the *JEDEC Standard JESD79-2C*.

NOTE 23: Input waveform timing is referenced from the input signal crossing at the $V_{IL(dc)}$ level for a rising signal and $V_{IH(dc)}$ for a falling signal applied to the device under test.

NOTE 29: These parameters are measured from a command/address signal (CKE, CS#, RAS#, CAS#, WE#, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/CK#) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

PASS Condition

The measured time interval between the address/control hold time and the respective clock crossing point should be within the specification limit.

Measurement Algorithm

1. Obtain the parameters and settings from the Configuration page.
2. Pre-condition the scope settings. Verify the actual DUT speed against the user speed selection at the Setup page.
3. Perform signal checking on all the signals in-use in the measurement to ensure that it can be triggered during the test. This includes Vp-p, Vmin, Vmax and Vmid of each signal.
4. Perform signal skew checking on the CK-DQS.
5. tIH measurement will compare the rising edge (address/control rising e.g. Vih_dc against associated clock crossing) OR falling edge (address/control falling e.g. Vil_dc against associated clock crossing).
6. Assign marker A for the clock signal while marker B for the data signal, for the final measurement result.
7. Measure delta of marker A and marker B and this will be the test result.
8. Compare the test result against the compliance test limit.

Test References

See Table 41 - Timing Parameters by Speed Grade (DDR2-400 and DDR2-533) and Table 42 - Timing Parameters by Speed Grade (DDR2-667 and DDR2-800), in the *JEDEC Standard JESD79-2C*.

12 Advanced Debug Mode Read-Write Eye-Diagram Tests

This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode Read-Write Eye-Diagram tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Advanced Debug Mode Read-Write Eye Diagram Tests

When performing the Advanced Debug Mode Read-Write Eye Diagram tests, the DDR2 Compliance Test Application will prompt you to make the proper connections as shown in Figure 76.

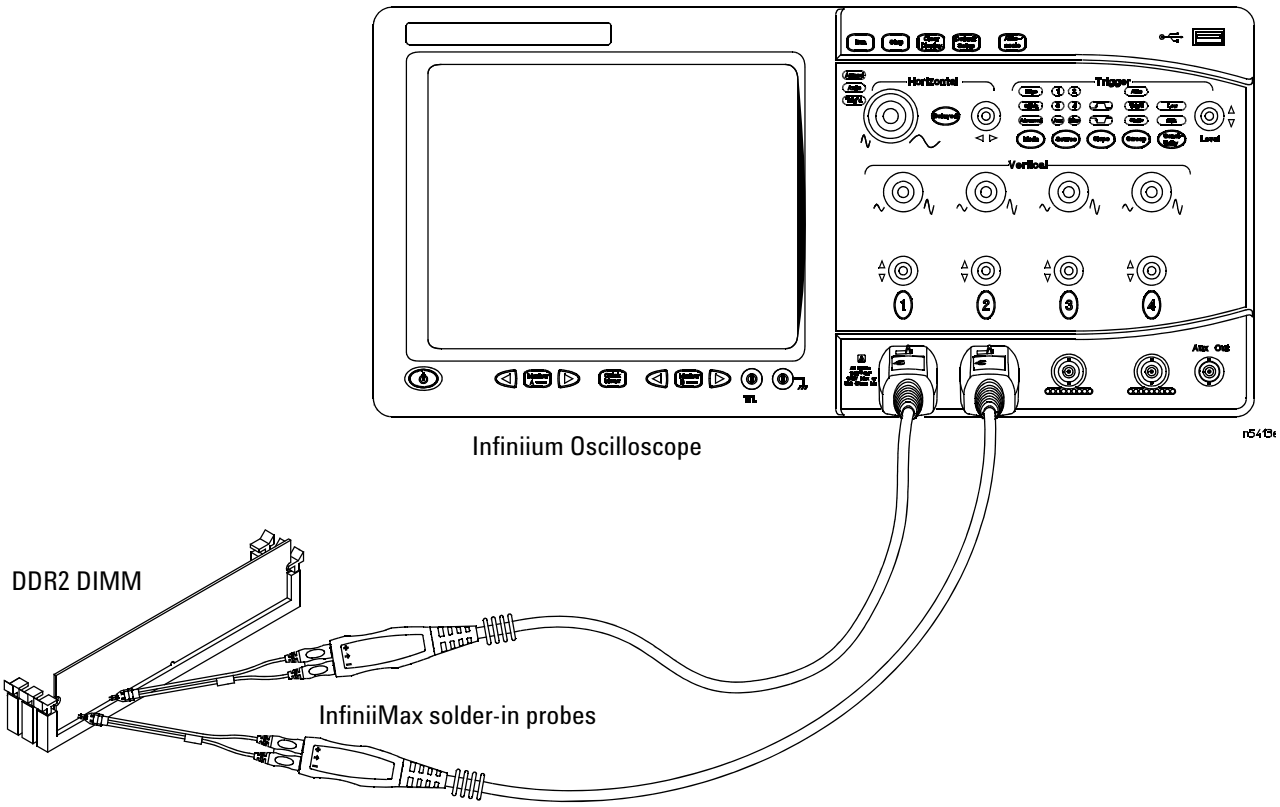

Figure 76 Probing for Advanced Debug Mode Read-Write Eye Diagram Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You can identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channels shown in Figure 76 are just examples).

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR2 Device Under Test (DUT) is attached. This software will perform a test on all the unused RAM on the system by producing repetitive bursts of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUTs on the DDR2 DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR2 Test application, click the Set Up tab.

6 Select Advanced Debug as the Test Mode option. This selection shows an additional command button - **Set Mask File**.

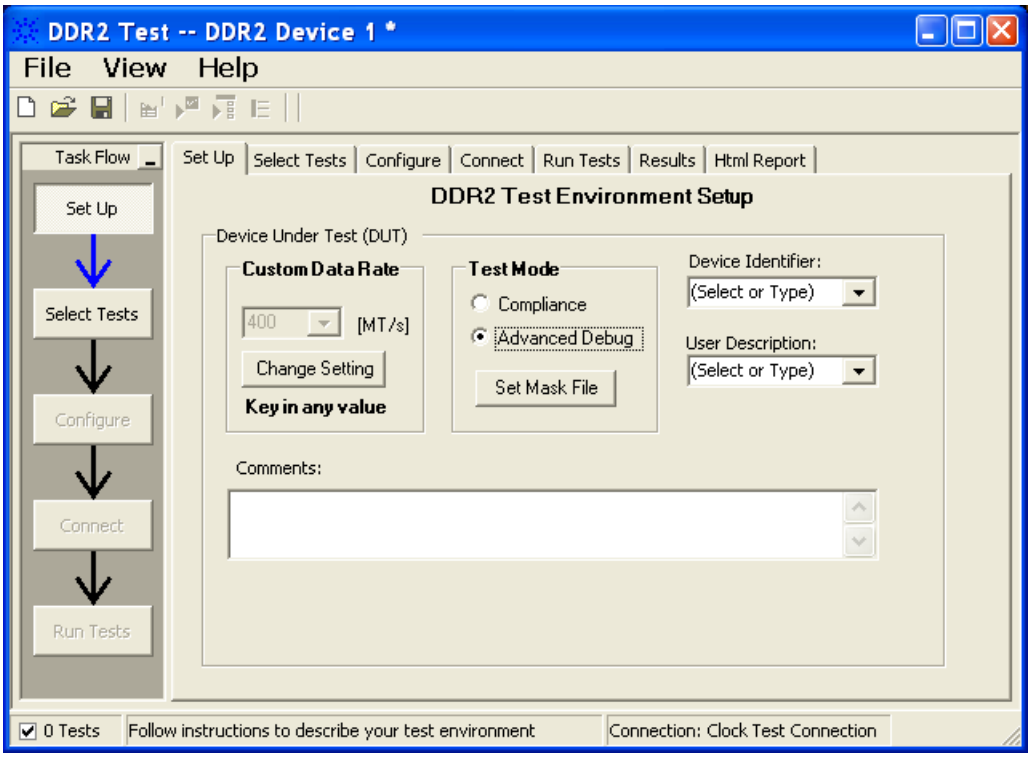

Figure 77 Selecting Advanced Debug Test Mode

7 Click this button to view or select test mask files for eye diagram tests.

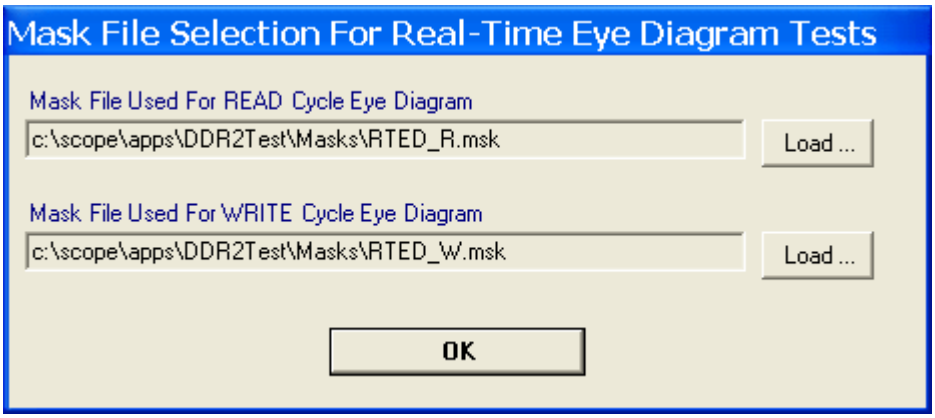

Figure 78 Selecting Test Mask for Eye Diagram Tests

8 Advanced Debug Mode also allows you to type in the data rate of the DUT signal.

9 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

10 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

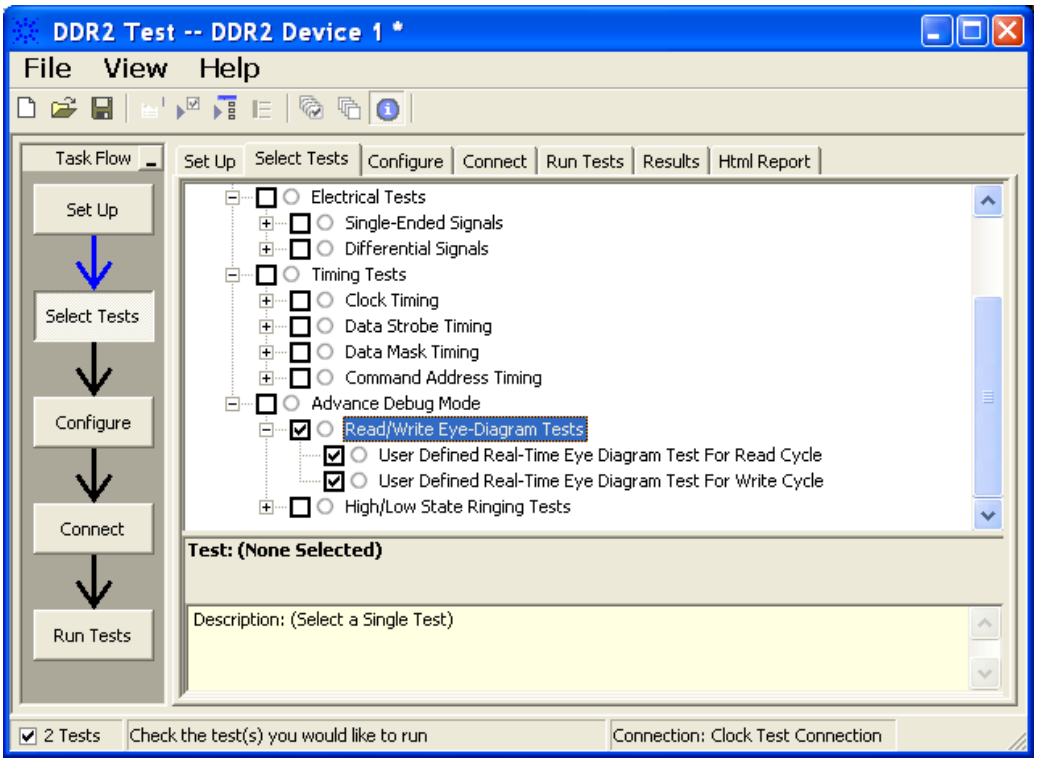

Figure 79 Selecting Advanced Debug Read-Write Eye-Diagram Tests

11 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 56), run the tests and view the tests results.

Table 56 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Advance Debug Mode	
Data Lane	Identifies the data lane for the eye diagram tests.
Data Source	Identifies the source of the data to be analyzed for eye diagram tests.
Data Strobe Lane	Identifies the data strobe lane for the eye diagram tests.
Data Strobe Source	Identifies the source of the data strobe for eye diagram tests.
Total Waveform	Select or type the total number of waveforms required for eye diagram tests.
Trigger Level	Identifies the rising edge voltage level to trigger on for the eye diagram tests.
Re-scale Test Mask	You may enable or disable the horizontal re-scaling option of the selected test mask.
InfiniiScan Limits	
Read Cycle	
IScan_UL_READ	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle).
IScan_LL_READ	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (READ cycle).
Write Cycle	
IScan_UL_WRITE	Identifies the upper limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle).

Configuration Option	Description
IScan_LL_WRITE	Identifies the lower limit for Setup Time measurement used in the InfiniiScan Measurement Mode (WRITE cycle).

User Defined Real-Time Eye Diagram Test for Read Cycle Method of Implementation

The Advanced Debug Mode Read-Write Eye Diagram test can be divided into two sub-tests. One of them is the User Defined Real-Time Eye Diagram Test for Read Cycle. There is no available specification on the eye test in *JEDEC Standard JESD79-2C* specifications. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR2 data READ cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

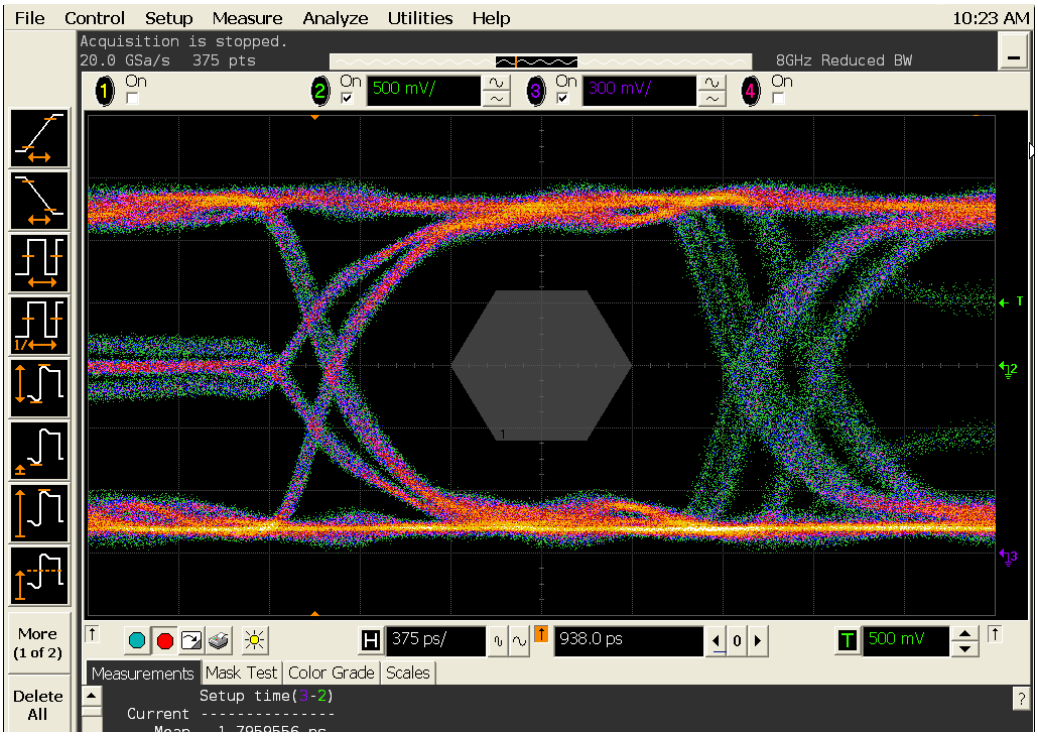

Figure 80 Eye Diagram Tests for Read Cycle

Signals of Interest

Based on the test definition (Read cycle only):

- Data Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)

- Data Strobe Signal (DQS as Supporting Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Measurement Algorithm

1. Set the termination condition of the mask test to "Waveforms" with the number of waveforms to be acquired.
2. Start mask test.
3. Loop until number of required waveforms are acquired.
4. Obtain and display total failed waveforms as the test result.

User Defined Real-Time Eye Diagram Test for Write Cycle Method of Implementation

Just as in the previous test, there is no available specification on the eye diagram test in the *JEDEC Standard JESD79-2C* specifications for User Defined Real-Time Eye Diagram Test for Write Cycle. Mask testing is definable by the customers for their evaluation tests purpose. The purpose of this test is to automate all the required setup procedures in order to generate an eye diagram for the DDR2 data WRITE cycle. This additional feature of mask test allows you to perform evaluation and debugging on the created eye diagram. The test will show a fail status if the total failed waveforms is greater than 0.

.

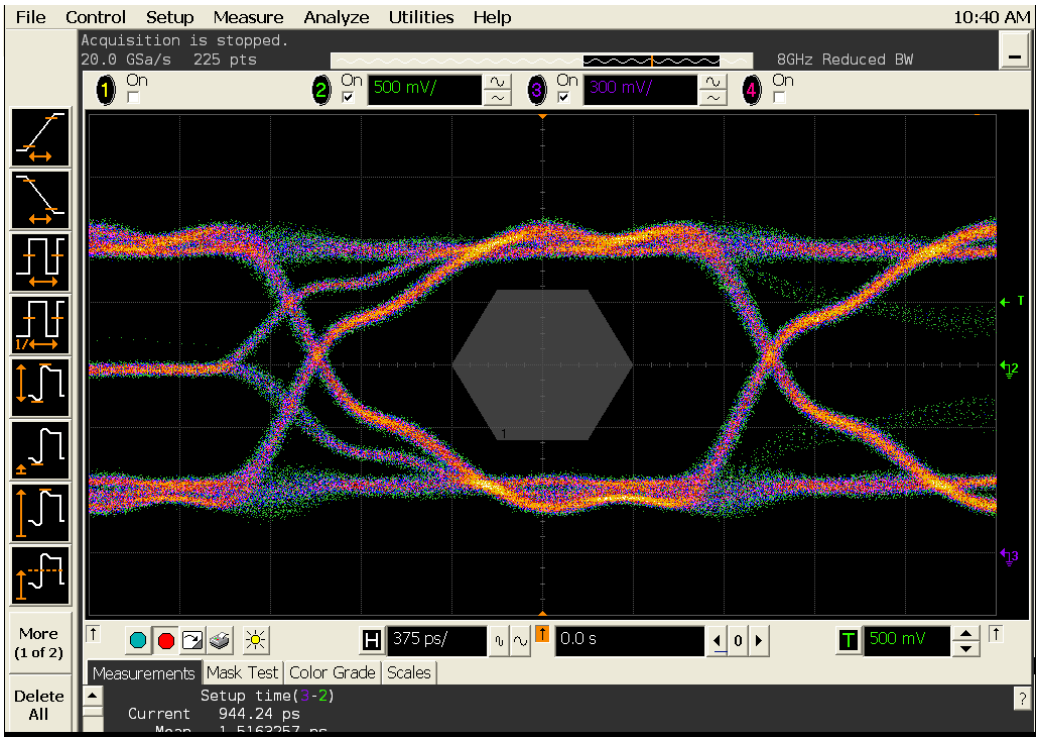

Figure 81 Eye Diagram Tests for Write Cycle

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signal

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Data Strobe Signal (DQS as Supporting Signal)

- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Measurement Algorithm

1. Set the termination condition of the mask test to "Waveforms" with the number of waveforms to be acquired.
2. Start mask test.
3. Loop until number of required waveforms are acquired.
4. Obtain and display total failed waveforms as the test result.

13 Advance Debug Mode High-Low State Ringing Tests

This section provides the Methods of Implementation (MOIs) for Advanced Debug Mode High-Low State Ringing tests using an Agilent 54850A series, 80000 or 90000A Series Infiniium oscilloscope, recommended InfiniiMax 116xA or 113xA probe amplifiers, E2677A differential solder-in probe head and the DDR2 Compliance Test Application.

Probing for Advanced Debug Mode High-Low State Ringing Tests

When performing the intra-pair skew tests, the DDR2 Compliance Test Application will prompt you to make the proper connections as shown in Figure 82.

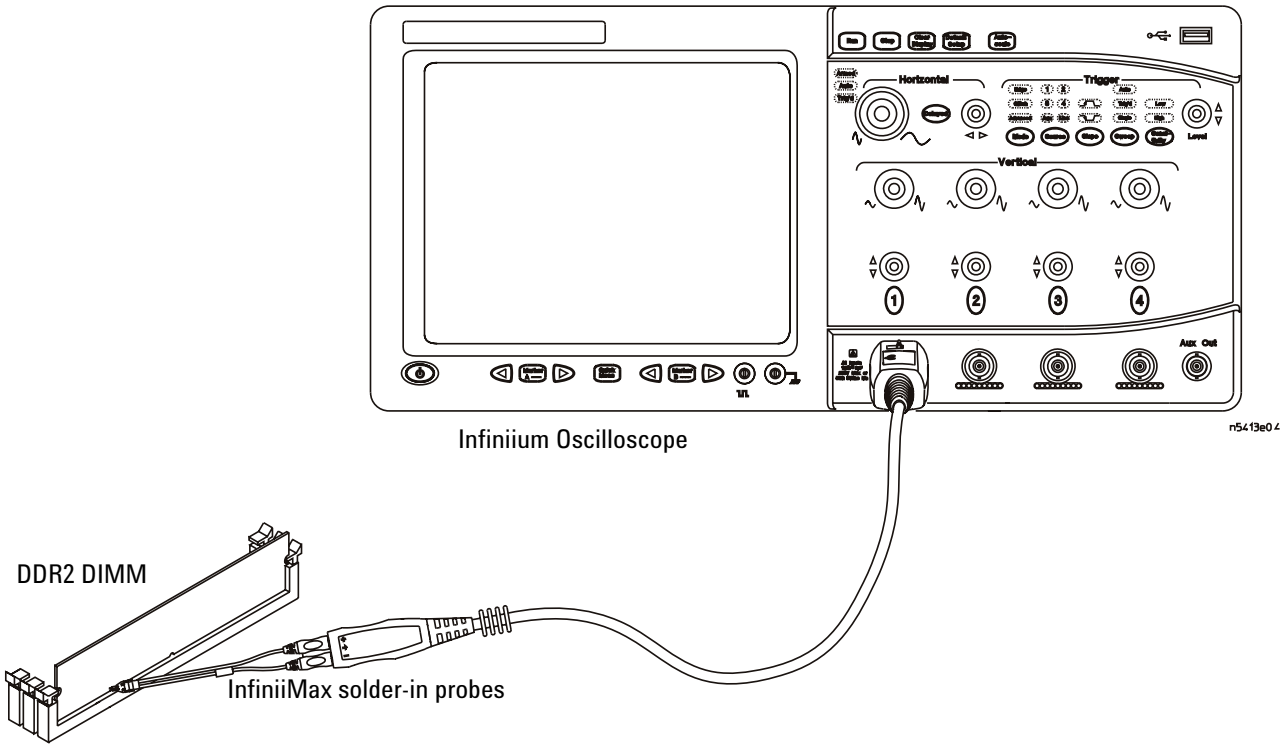

Figure 82 Probing for Advanced Debug Mode High-Low State Ringing Tests

You can use any of the oscilloscope channels as the Pin Under Test (PUT) source channel. You identify the channels used for each signal in the Configuration tab of the DDR2 Compliance Test Application. (The channel shown in Figure 82 is just an example.)

For more information on the probe amplifiers and differential probe heads, see Chapter 15, “InfiniiMax Probing,” starting on page 251.

Test Procedure

1 Start the automated test application as described in "Starting the DDR2 Compliance Test Application" on page 27.

2 Ensure that the RAM reliability test software is running on the computer systems where the DDR2 Device Under Test (DUT) is attached. This software will perform tests on all the unused RAM in the system by producing repetitive bursts of read-write data signals to the DDR2 memory.

3 Connect the differential solder-in probe head to the PUT on the DDR2 DIMM.

4 Connect the oscilloscope probes to any of the oscilloscope channels.

5 In the DDR2 test application, click the Set Up tab.

6 Select Advanced Debug as the Test Mode option. This selection shows an additional command button - **Set Mask File**. This is only relevant for Read-Write Eye-Diagram.

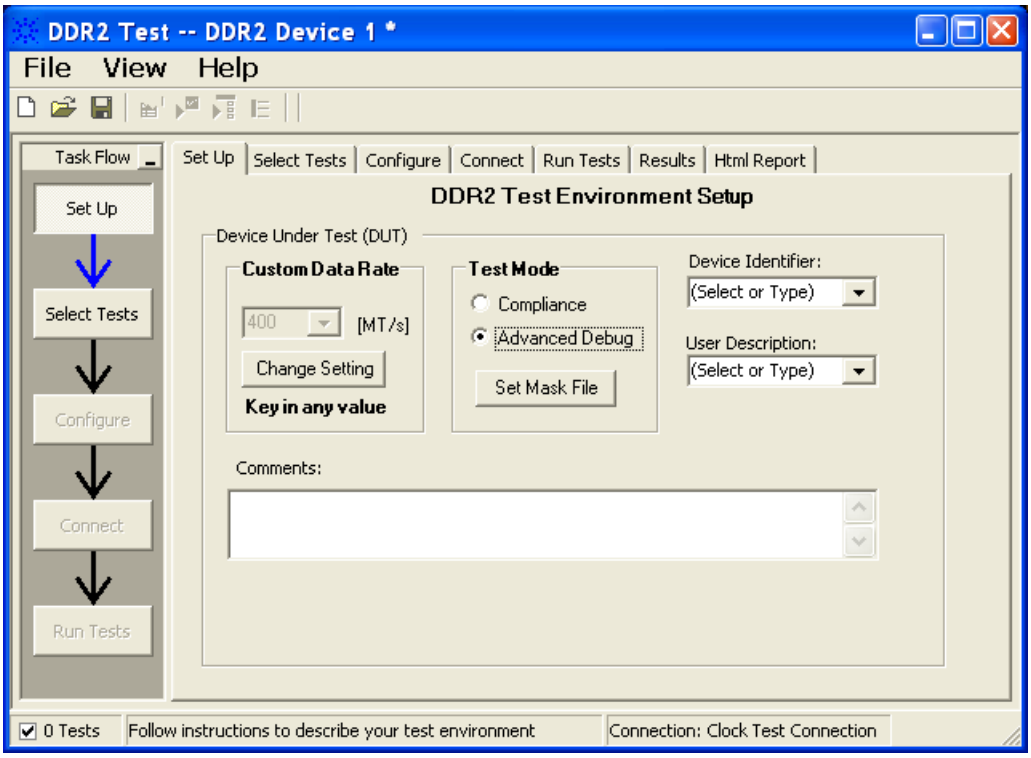

Figure 83 Selecting Advanced Debug Test Mode

7 Advanced Debug Mode also allows you to type in the data rate of the DUT signal.

8 Type in or select the Device Identifier as well as the User Description from the drop-down list. Enter your comments in the Comments text box.

9 Click the Select Tests tab and check the tests you want to run. Check the parent node or group to check all the available tests within the group.

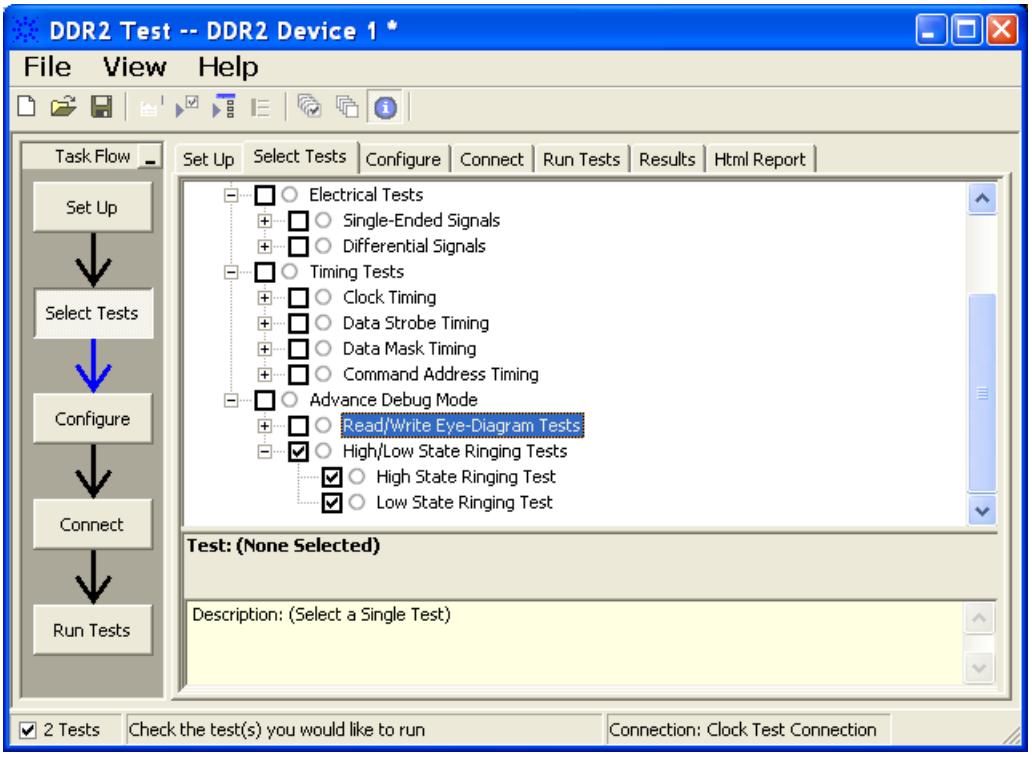

Figure 84 Selecting Advanced Debug High-Low State Ringing Tests

10 Follow the DDR2 Test application's task flow to set up the configuration options (see Table 57), run the tests and view the tests results.

Table 57 Test Configuration Options

Configuration Option	Description
Stop on error	Enabling this option will allow error messages to prompt whenever the test criteria is not met. Disabling this option will allow the system to bypass all the error messages that could occur and proceed to the next test. This option is suitable for long hours multiple trials.
Signal Threshold setting by percentage	This option allows you to define the Upper and Lower threshold of the signal by percentage.
VDD	Input supply voltage value.
VDDQ	Input supply voltage for data output.
Vref	Input reference voltage value.
Vih(DC)	Input voltage high value (direct current).
Vih(AC)	Input voltage high value (alternating current).
Vil(DC)	Input voltage low value (direct current).
Vil(AC)	Input voltage low value (alternating current).
Advance Debug Mode	
Pin Under Test, PUT	Identifies the Pin Under Test for High/Low State Ringing tests
PUT Source	Identifies the source of the PUT for High-Low State Ringing tests.
Time-out	Identifies the time-out value to be used for High-Low State Ringing Tests.
Trigger Level	Sets the rising edge voltage level to trigger on for all High-Low State Ringing Tests.
Upper Level	Identifies the upper threshold level to be used for the ringing tests.
Hysteresis	Identifies the hysteresis value to be used for the ringing tests.
Lower Level	Identifies the lower threshold level to be used for the ringing tests.

High State Ringing Tests Method of Implementation

The Advanced Debug Mode Ringing test can be divided into two sub-tests. One of them is the High State Ringing test. There is no available specification for this test in the *JEDEC Standard JESD79-2C* specifications. The ringing debug test is definable by the customers to capture the glitch of interest for the logic high state section in a test signal for evaluation purposes. The purpose of this test is to automate all the required setup procedures, particularly the InfiniiScan RUNT mode setup, to capture the ringing section of a test signal. Users are required to customize the threshold value in the Configure tab to capture the specific RUNT signals. The expected results are signals captured on the screen that fulfill the InfiniiScan RUNT criteria. There is a pulse in the captured signal that passes through two voltage level threshold but not the third.

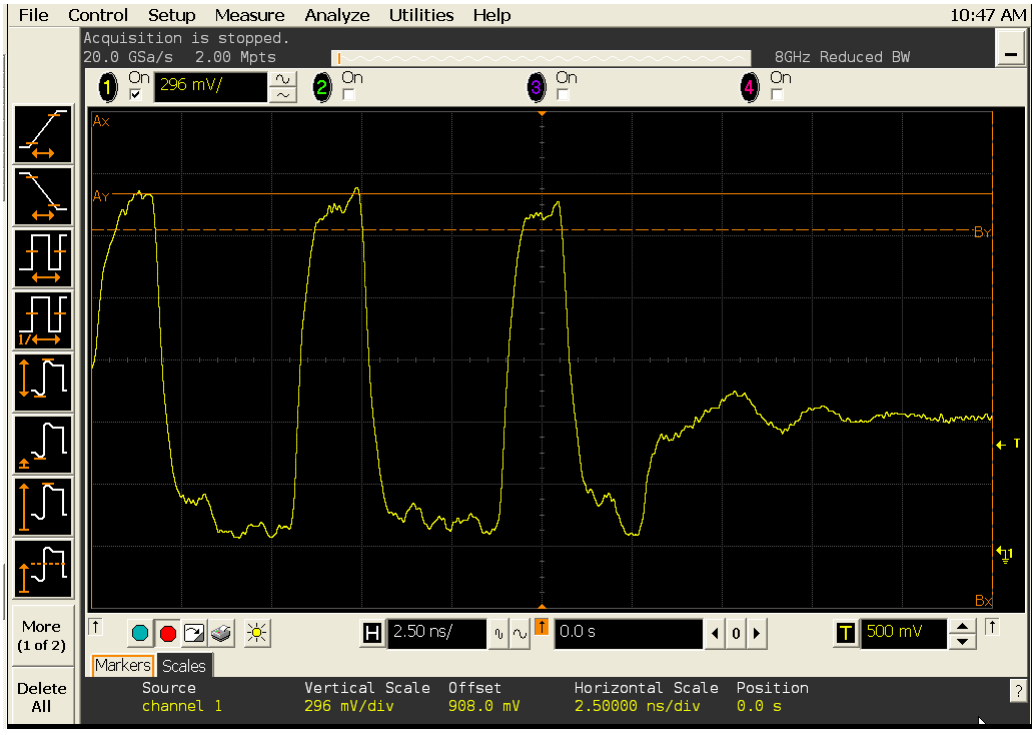

Figure 85 High State Ringing Test

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against the user's speed grade selection

Measurement Algorithm

1. Acquire initial signal data and then perform signal conditioning to maximize the screen resolution - vertical scale adjustment.
2. Setup the InfiniiScan to activate the RUNT mode.
3. Acquire test data with the InfiniiScan RUNT activated.
4. Display Markers to show the RUNT Upper Level and RUNT Lower Level.

Low State Ringing Tests Method of Implementation

Just as the High State Ringing test, there is no available specification in the *JEDEC Standard JESD79-2C* specifications for the Low State Ringing tests. The ringing debug test is definable by the customers to capture the glitch of interest for the logic low state section in a test signal for evaluation purposes. The purpose of this test is to automate all the required setup procedures, particularly the InfiniiScan RUNT mode setup, to capture the ringing section of a test signal. Users are required to customize the threshold value in the Configure tab to capture the specific RUNT signals. The expected results are signals captured on the screen that fulfill the InfiniiScan RUNT criteria. There is a pulse in the captured signal that passes through two voltage level threshold but not the third.

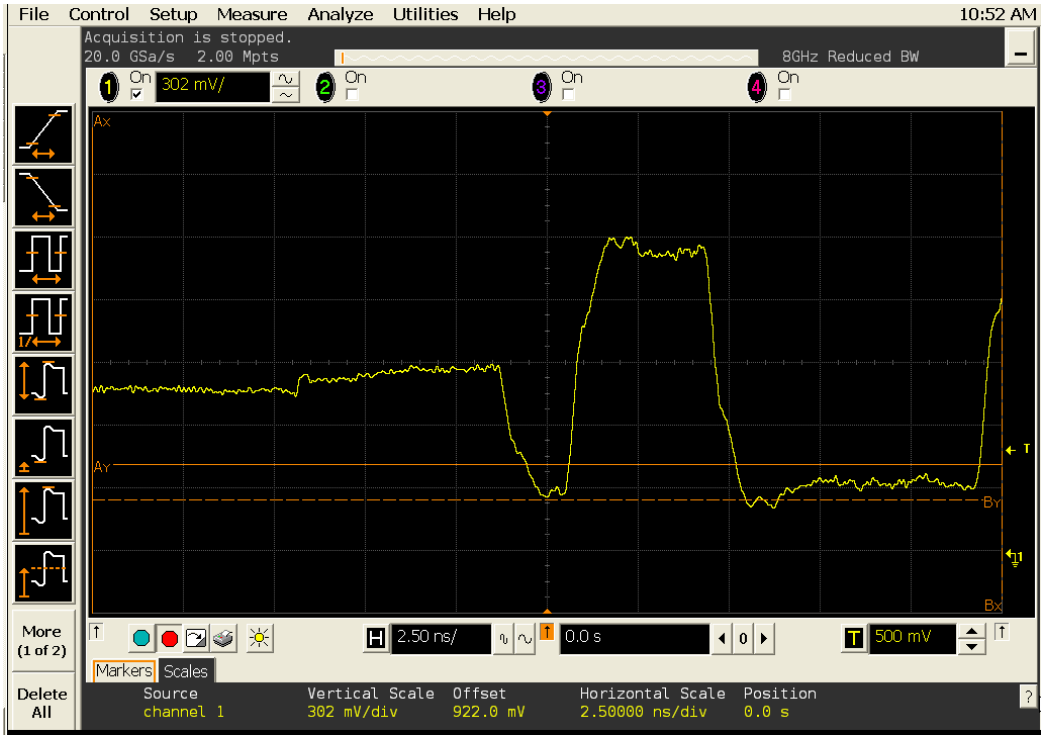

Figure 86 Low State Ringing Test

Signals of Interest

Based on the test definition (Write cycle only):

- Data Signals OR
- Data Strobe Signals OR
- Address Signals OR
- Control Signal OR
- Data Mask Control Signals

Signals required to perform the test on the oscilloscope:

- Data Signal (DQ as Pin Under Test Signal)
- Clock Signal - CK is required to perform pre-test to verify the DUT speed against user's speed grade selection

Measurement Algorithm

1. Acquire initial signal data and then perform signal conditioning to maximize the screen resolution - vertical scale adjustment.
2. Setup the InfiniiScan to activate the RUNT mode.
3. Acquire test data with the InfiniiScan RUNT activated.
4. Display Markers to show the RUNT Upper Level and RUNT Lower Level.

14 Calibrating the Infiniium Oscilloscope and Probe

This section describes the Agilent Infiniium digital storage oscilloscope calibration procedures.

Required Equipment for Oscilloscope Calibration

To calibrate the Infiniium oscilloscope in preparation for running the DDR2 automated tests, you need the following equipment:

- Keyboard, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Agilent Infiniium oscilloscope).
- Precision 3.5 mm BNC to SMA male adapter, Agilent p/n 54855-67604, qty = 2 (provided with the Agilent Infiniium oscilloscope).
- Calibration cable (provided with the 54850A series , 80000 and 90000A series Infiniium oscilloscopes). Use a good quality 50 Ω BNC cable.
- BNC shorting cap (provided with the 54850A series Infiniium oscilloscopes).

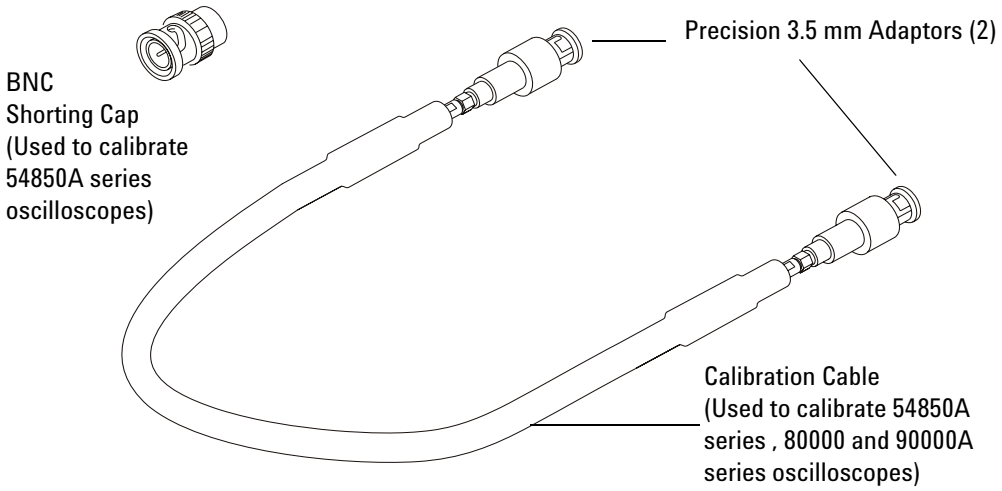

Figure 87 Accessories Provided with the Agilent Infiniium Oscilloscope

Internal Calibration

This will perform an internal diagnostic and calibration cycle for the oscilloscope. For the Agilent oscilloscope, this is referred to as Calibration. This Calibration will take about 20 minutes. Perform the following steps:

1 Set up the oscilloscope with the following steps:

   a Connect the keyboard, mouse, and power cord to the rear of the oscilloscope.

   b Plug in the power cord.

   c Turn on the oscilloscope by pressing the power button located on the lower left of the front panel.

   d Allow the oscilloscope to warm up at least 30 minutes prior to starting the calibration procedure in step 3 below.

2 Locate and prepare the accessories that will be required for the internal calibration:

   a Locate the BNC shorting cap.

   b Locate the calibration cable.

   c Locate the two Agilent precision SMA/BNC adapters.

   d Attach one SMA adapter to the other end of the calibration cable - hand tighten snugly.

   e Attach another SMA adapter to the other end of the calibration cable - hand tighten snugly.

3 Referring to Figure 88 below, perform the following steps:

   a Click on the Utilities>Calibration menu to open the Calibration dialog box.

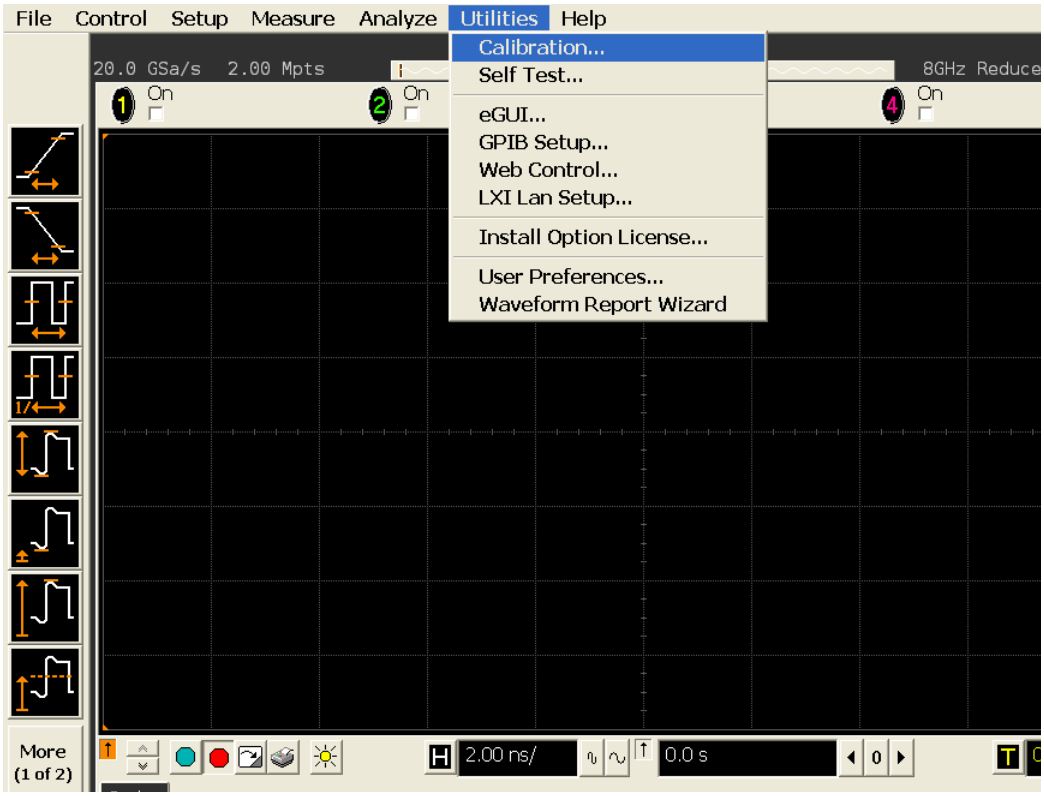

Figure 88 Accessing the Calibration Menu

4 Referring to Figure 89 below, perform the following steps to start the calibration:

   b Uncheck the Cal Memory Protect checkbox.

   c Click the Start button to begin the calibration.

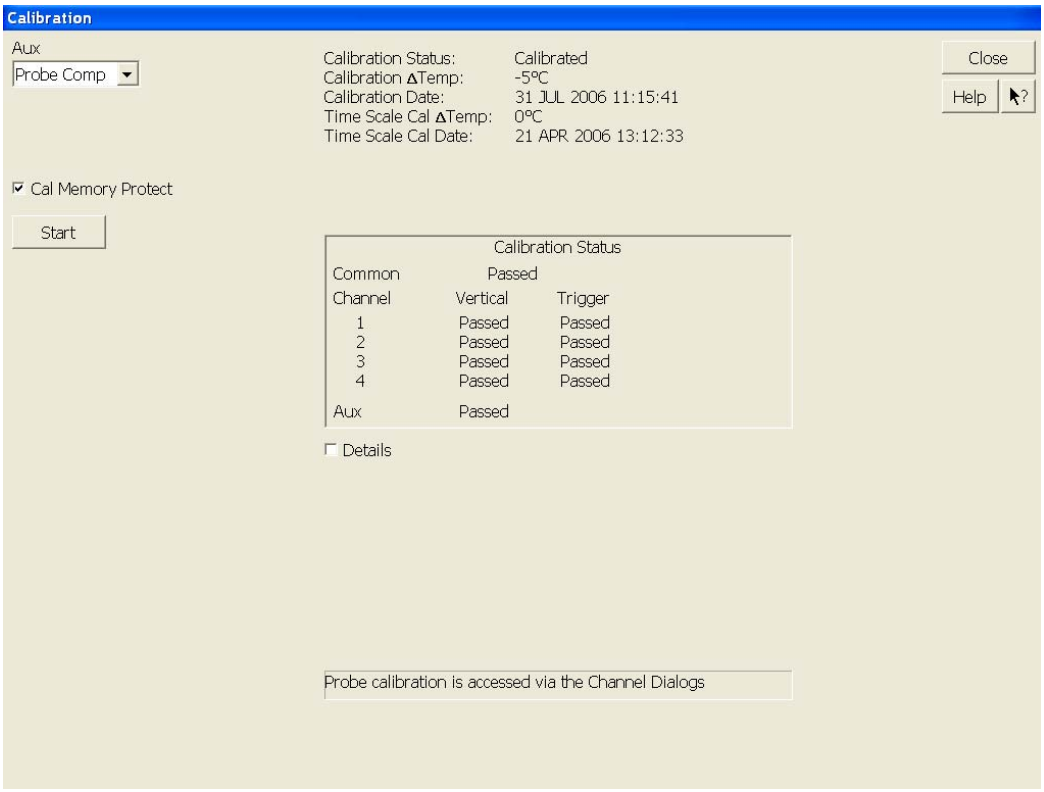

Figure 89 Oscilloscope Calibration Window

d During the calibration of channel 1, if you are prompted to perform a Time Scale Calibration, as shown in Figure 90 below.

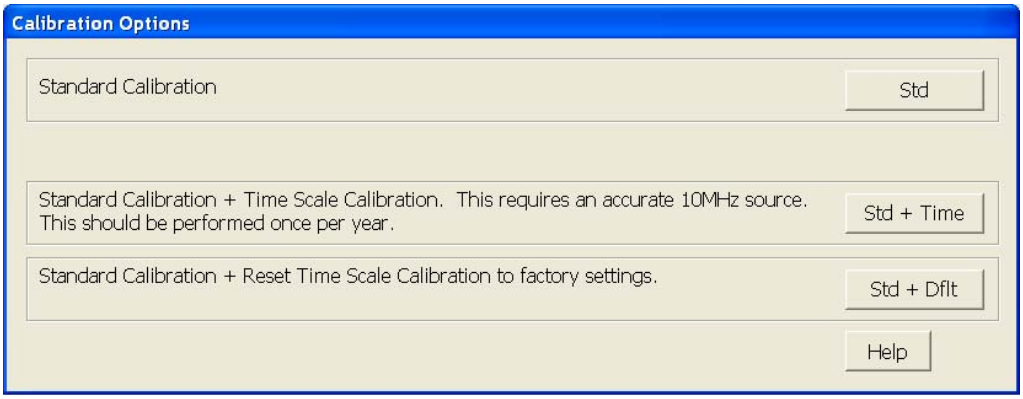

Figure 90 Time Scale Calibration Dialog box

e Click on the Std+Dflt button to continue the calibration, using the Factory default calibration factors.

f When the calibration procedure is complete, you will be prompted with a Calibration Complete message window. Click the OK button to close this window.

g Confirm that the Vertical and Trigger Calibration Status for all Channels passed.

h Click the Close button to close the calibration window.

i The internal calibration is completed.

j Read NOTE below.

NOTE These steps do not need to be performed every time a test is run. However, if the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, this calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the Utilities>Calibration menu.

Required Equipment for Probe Calibration

Before performing DDR2 tests you should calibrate the probes. Calibration of the solder-in probe heads consist of a vertical calibration and a skew calibration. The vertical calibration should be performed before the skew calibration. Both calibrations should be performed for best probe measurement performance.

The calibration procedure requires the following parts.

- BNC (male) to SMA (male) adaptor
- Deskew fixture
- 50 Ω SMA terminator

Probe Calibration

Connecting the Probe for Calibration

For the following procedure, refer to Figure 91 below.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the 50 Ω SMA terminator to the connector farthest from yellow pincher.
3. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
4. Connect the probe to an oscilloscope channel.
5. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
6. Push down the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
7. Release the yellow pincher.

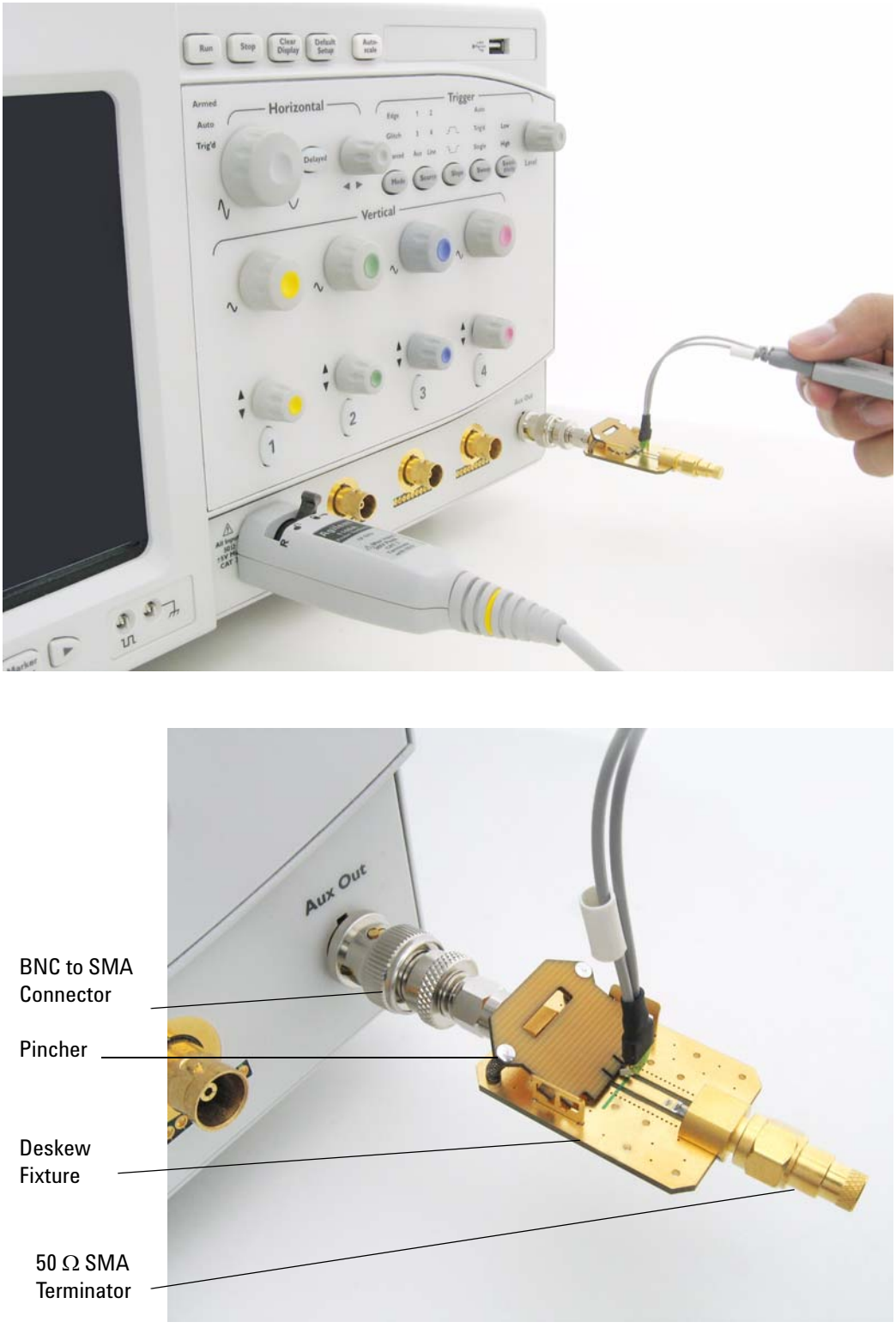

Figure 91 Solder-in Probe Head Calibration Connection Example

Verifying the Connection

1 On the Infiniium oscilloscope, press the autoscale button on the front panel.

2 Set the volts per division to 100 mV/div.

3 Set the horizontal scale to 1.00 ns/div.

4 Set the horizontal position to approximately 3 ns. You should see a waveform similar to that in Figure 92 below.

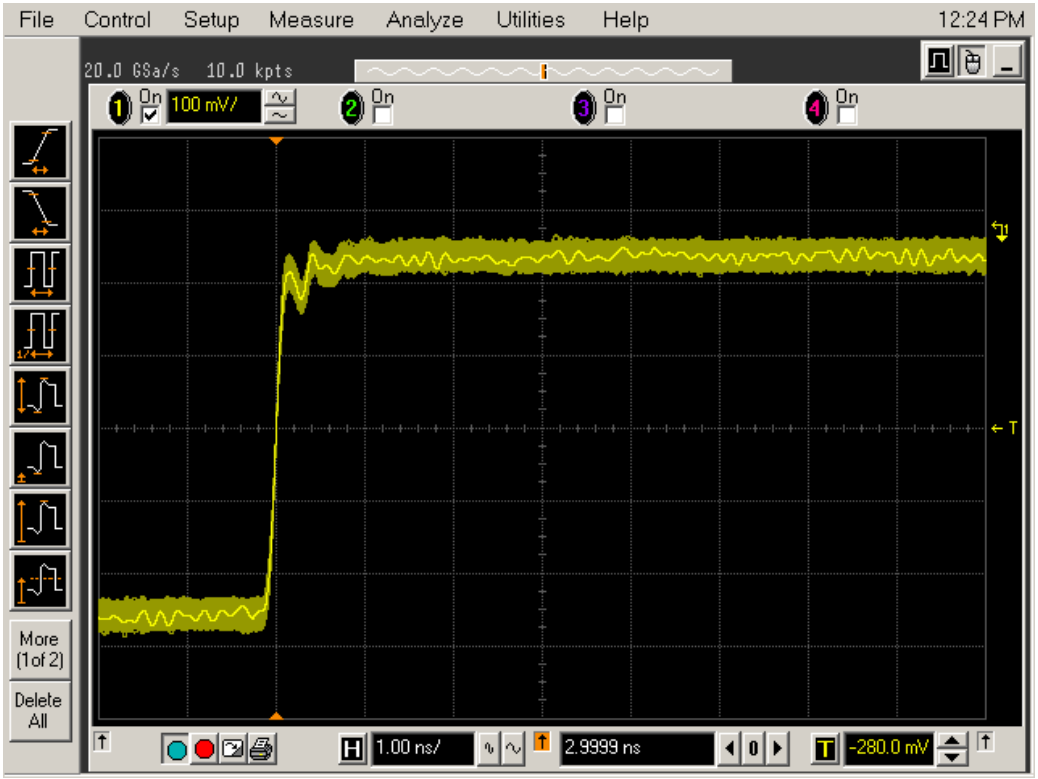

Figure 92 Good Connection Waveform Example

If you see a waveform similar to that of Figure 93 below, then you have a bad connection and should check all of your probe connections.

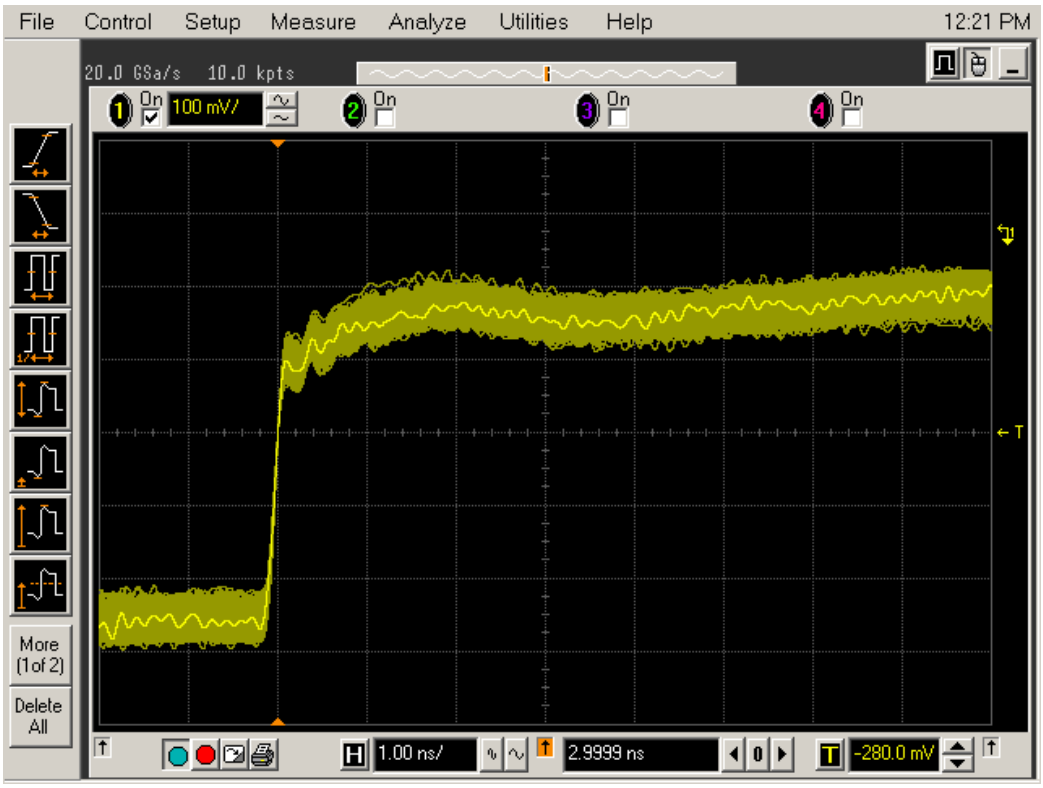

Figure 93 Bad Connection Waveform Example

Running the Probe Calibration and Deskew

1 On the Infiniium oscilloscope in the Setup menu, select the channel connected to the probe, as shown in Figure 94.

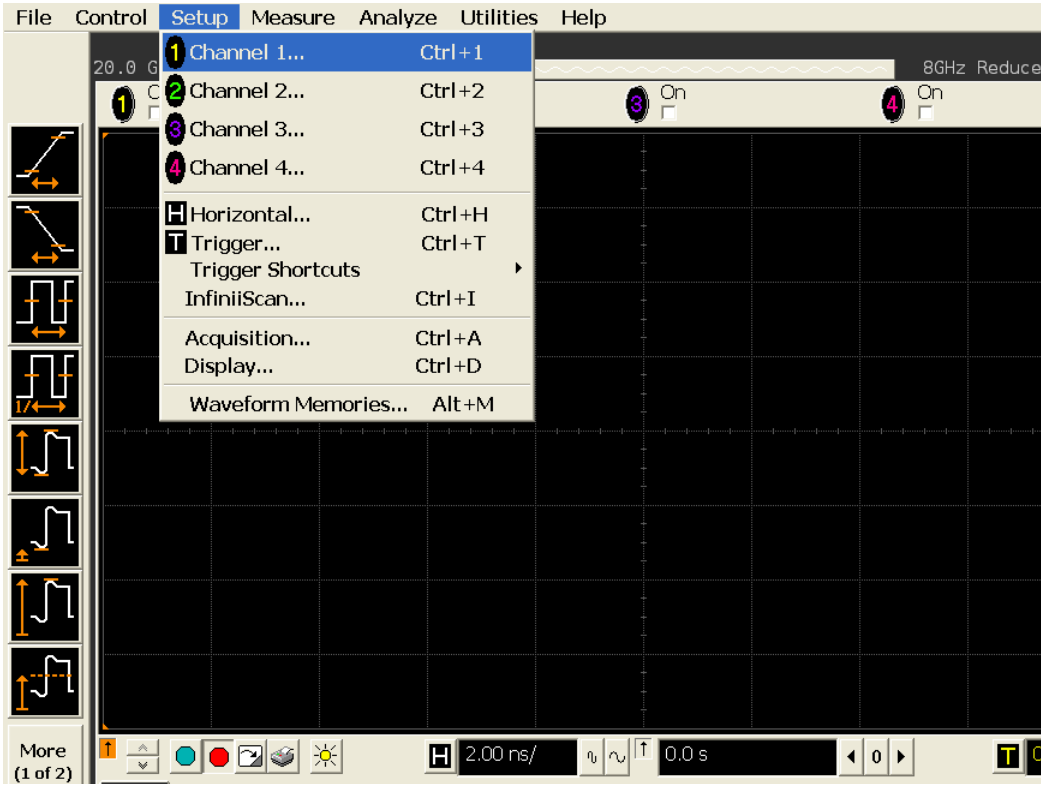

Figure 94 Channel Setup Window.

2 In the Channel Setup dialog box, select the Probes... button, as shown in Figure 95.

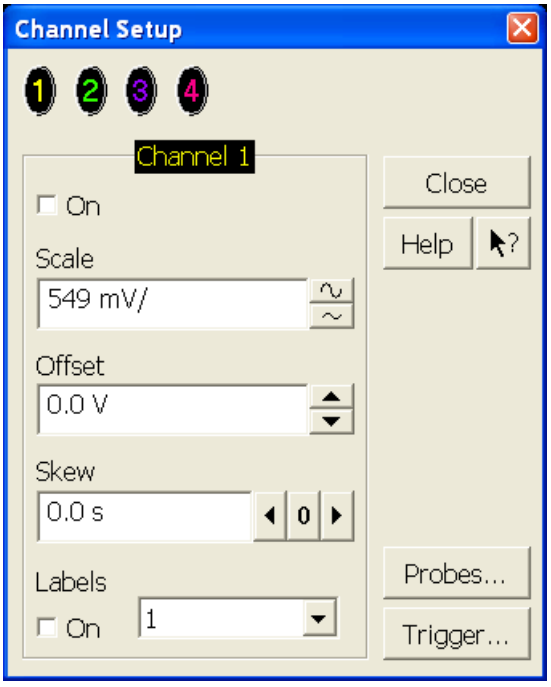

Figure 95 Channel Dialog Box

3 In the Probe Setup dialog box, select the Calibrate Probe... button.

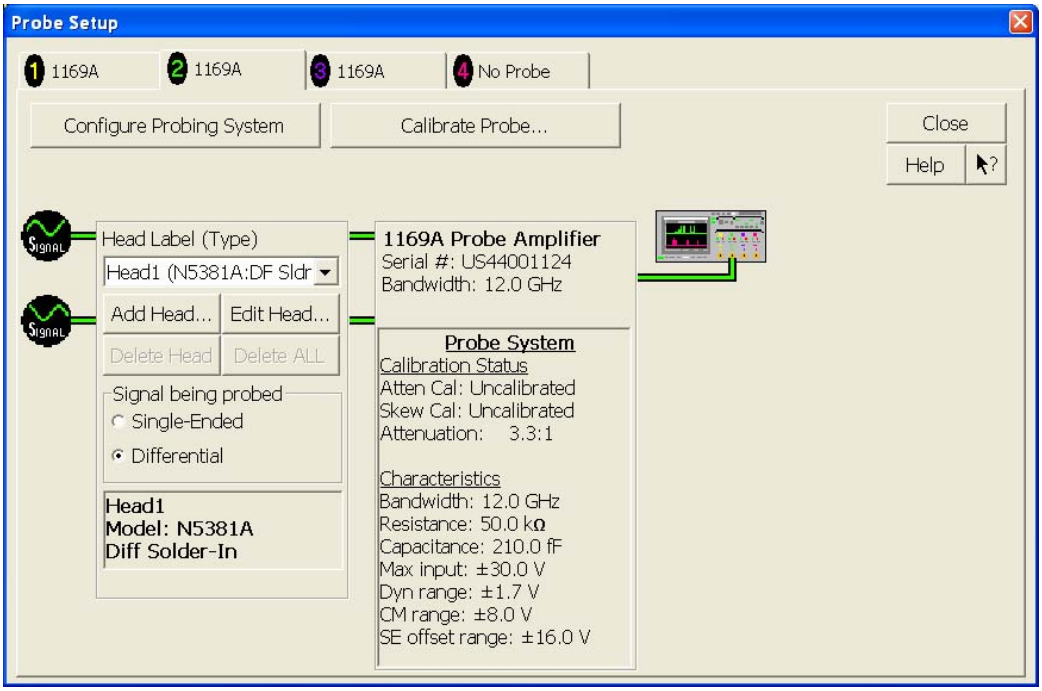

Figure 96 Probe Setup Window.

4 In the Probe Calibration dialog box, select the Calibrated Atten/Offset radio button.

5 Select the Start Atten/Offset Calibration... button and follow the on-screen instructions for the vertical calibration procedure.

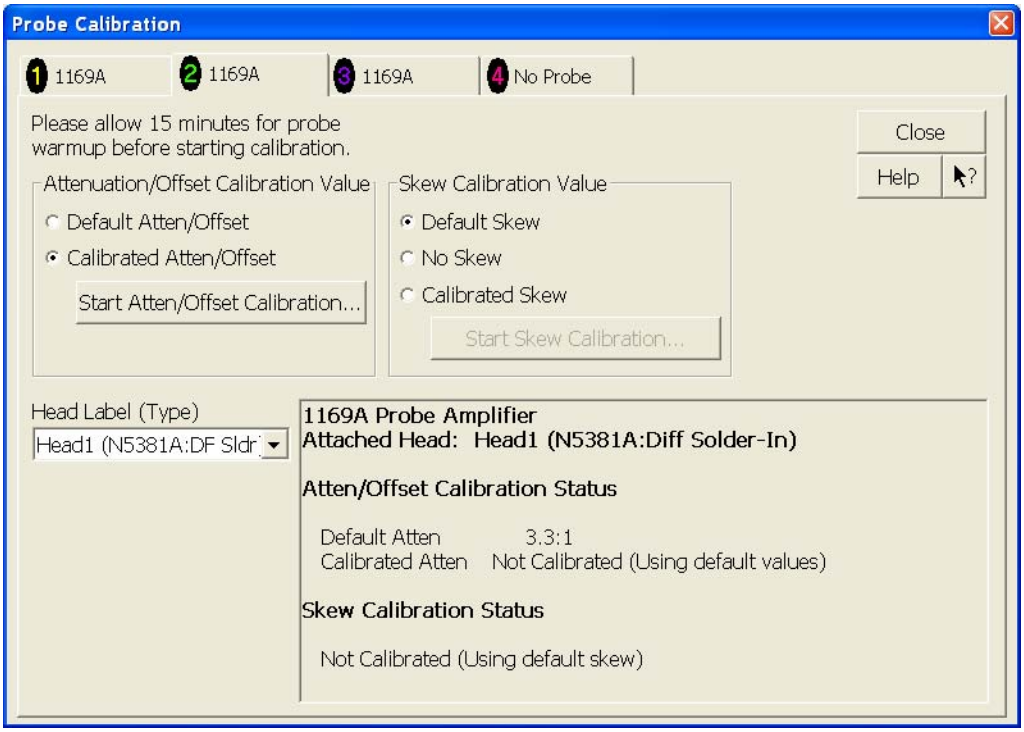

Figure 97 Probe Calibration Window.

6 Once the vertical calibration has successfully completed, select the Calibrated Skew... button.

7 Select the Start Skew Calibration... button and follow the on-screen instructions for the skew calibration.

At the end of each calibration, the oscilloscope will prompt you if the calibration was or was not successful.

Verifying the Probe Calibration

If you have successfully calibrated the probe, it is not necessary to perform this verification. However, if you want to verify that the probe was properly calibrated, the following procedure will help you verify the calibration.

The calibration procedure requires the following parts:

- BNC (male) to SMA (male) adaptor
- SMA (male) to BNC (female) adaptor
- BNC (male) to BNC (male) 12 inch cable such as the Agilent 8120-1838
- Agilent 54855-61620 calibration cable (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Agilent 54855-67604 precision 3.5 mm adaptors (Infiniium oscilloscopes with bandwidths of 6 Ghz and greater only)
- Deskew fixture

For the following procedure, refer to Figure 98.

1. Connect BNC (male) to SMA (male) adaptor to the deskew fixture on the connector closest to the yellow pincher.
2. Connect the SMA (male) to BNC (female) to the connector farthest from the yellow pincher.
3. Connect the BNC (male) to BNC (male) cable to the BNC connector on the deskew fixture to one of the unused oscilloscope channels. For infiniium oscilloscopes with bandwidths of 6 GHz and greater, use the 54855-61620 calibration cable and the two 54855-64604 precision 3.5 mm adaptors.
4. Connect the BNC side of the deskew fixture to the Aux Out BNC of the Infiniium oscilloscope.
5. Connect the probe to an oscilloscope channel.
6. To minimize the wear and tear on the probe head, it should be placed on a support to relieve the strain on the probe head cables.
7. Push down on the back side of the yellow pincher. Insert the probe head resistor lead underneath the center of the yellow pincher and over the center conductor of the deskew fixture. The negative probe head resistor lead or ground lead must be underneath the yellow pincher and over one of the outside copper conductors (ground) of the deskew fixture. Make sure that the probe head is approximately perpendicular to the deskew fixture.
8. Release the yellow pincher.
9. On the oscilloscope, press the autoscale button on the front panel.
10. Select Setup menu and choose the channel connected to the BNC cable from the pull-down menu.
11. Select the Probes... button.
12. Select the Configure Probe System button.
13. Select User Defined Probe from the pull-down menu.
14. Select the Calibrate Probe... button.

15 Select the Calibrated Skew radio button.

16 Once the skew calibration is completed, close all dialog boxes.

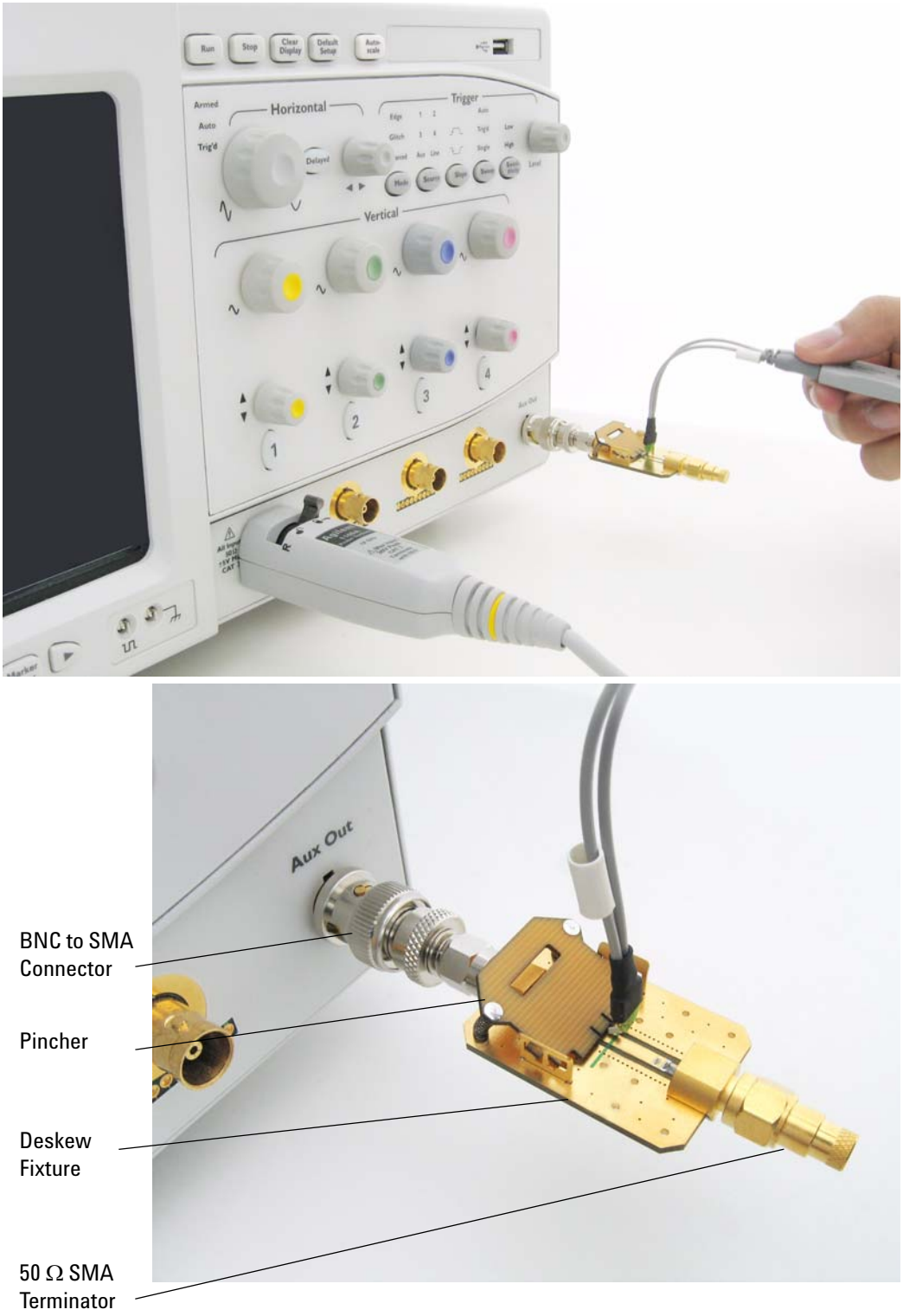

Figure 98 Probe Calibration Verification Connection Example

17 Select the Start Skew Calibration... button and follow the on-screen instructions.

18 Set the vertical scale for the displayed channels to 100 mV/div.

19 Set the horizontal range to 1.00 ns/div.

20 Set the horizontal position to approximately 3 ns.

21 Change the vertical position knobs of both channels until the waveforms overlap each other.

22 Select the Setup menu choose Acquisition... from the pull-down menu.

23 In the Acquisition Setup dialog box enable averaging. When you close the dialog box, you should see waveforms similar to that in Figure 99.

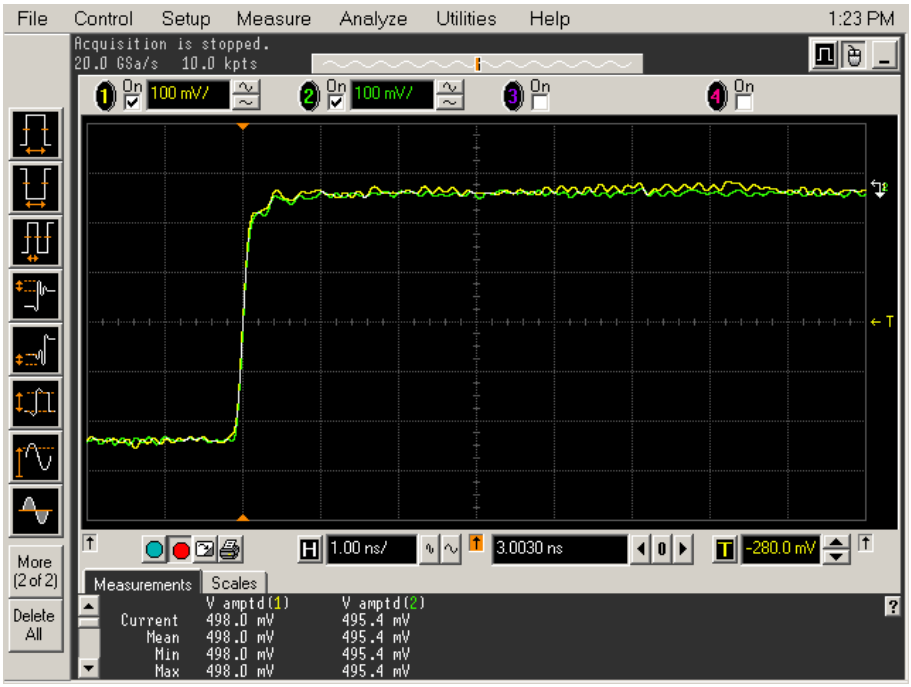

Figure 99 Calibration Probe Waveform Example

NOTE

Each probe is calibrated with the oscilloscope channel to which it is connected. Do not switch probes between channels or other oscilloscopes, or it will be necessary to calibrate them again. It is recommended that the probes be labeled with the channel on which they were calibrated.

15 InfiniiMax Probing

Figure 100 1134A InfiniiMax Probe Amplifier

Agilent recommends 116xA or 113xA probe amplifiers, which range from 3.5 GHz to 12 GHz.

Agilent also recommends the E2677A differential solder-in probe head. Other probe head options include N5381A InfiniiMax II 12 GHz differential solder-in probe head, N5382A InfiniiMax II 12 GHz differential browser, E2675A InfiniiMax differential browser probe head, N5425A InfiniiMax ZIF probe head and N5426A ZIF Tips.

Figure 101 E2677A / N5381A Differential Solder-in Probe Head

Table 58 Probe Head Characteristics (with 1134A probe amplifier)

Probe Head	Model Number	Differential Measurement (BW, input C, input R)	Single-Ended Measurement (BW, input C, input R)
Differential Solder-in	E2677A	7 GHz, 0.27 pF, 50 kOhm	7 GHz, 0.44 pF, 25 kOhm

Used with 1168A or 1169A probe amplifier, the E2677A differential solder-in probe head provides 10 GHz and 12 GHz bandwidth respectively.

16 Common Error Messages

When performing DDR tests, error message dialog boxes can occur due to improper configuration settings. This section describes the common errors, causes and solution to the problem.

Required Triggering Condition Not Met

The following error message will appear when a time-out occurs. This error message indicates that the required triggering condition is not met. This is followed by test cancellation and aborting message. All pending tests will be cancelled.

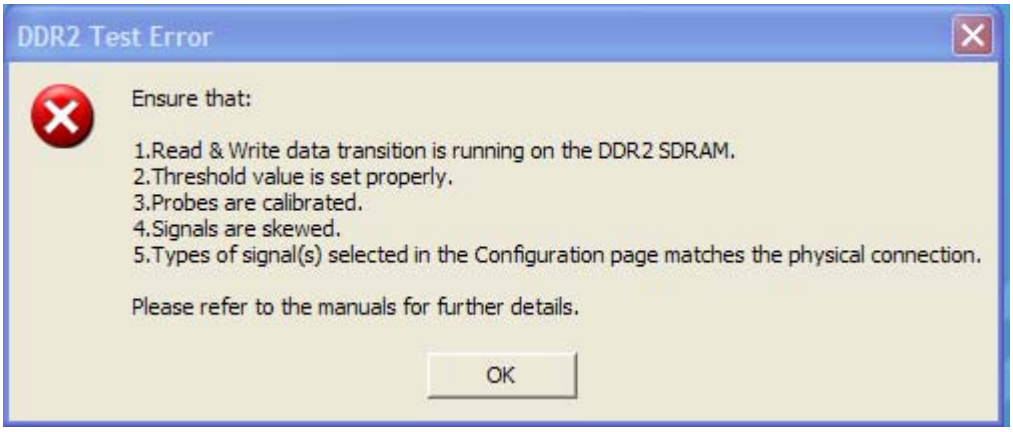

Figure 102 Required Trigger Condition Not Met Error Message

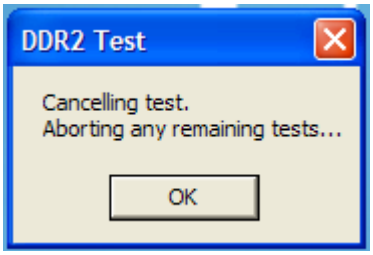

Figure 103 Cancel and Abort Test Message

These error dialog boxes appear when one of the following configuration errors is encountered.

- Required triggering condition is not met. For example, if the setup time condition in a triggering requirement, is not met within a certain time (approximately 10s), the time-out error will occur.
- Attempt to run the Electrical tests without first executing the RAM reliability test software on the DDR2 Device Under Test (DUT) system.
- Attempt to run the Electrical tests without providing any test signal to the oscilloscope.
- Threshold value is not properly set.
- Signals are not skewed.

- The type of signals selected in the Configuration page does not match the physical connection.

Ensure that:

- The RAM reliability test software is running to exercise the SDRAM. This ensures that there are Read and Write signals running on the SDRAM in order for the application to capture the signal.
- The threshold is properly set according to the actual signal performance. For example, if the maximum voltage of the DQ signal is 1.8V and the minimum voltage is 40mV, you must ensure that the upper and lower threshold value does not exceed the minimum and maximum limit, in order to trigger the signal. Scope will not be triggered if the upper threshold is set to be above 1.8V, since the maximum voltage on the actual signal is just 1.8V and below.
- The probes are properly calibrated and skewed. Ensure that correct probes are used and they are properly calibrated, so that it reflects the actual signal and is not over or under amplified. Similarly, ensure that the channels are properly soldered on the DDR module and ensure that the signals are not over skewed.
- The types of signals selected in the Configuration page matches the physical connection. For example, if Channel 1 is physically connected to the Clock signal, ensure that you select the same in the Configuration page.

Software License Error

When you load the N5413A DDR2 Compliance Test Application, it checks for the required software licenses. When one of the optional licenses is not detected, the application will limit the available test options and the Set Up tab will look similar to following screenshot.

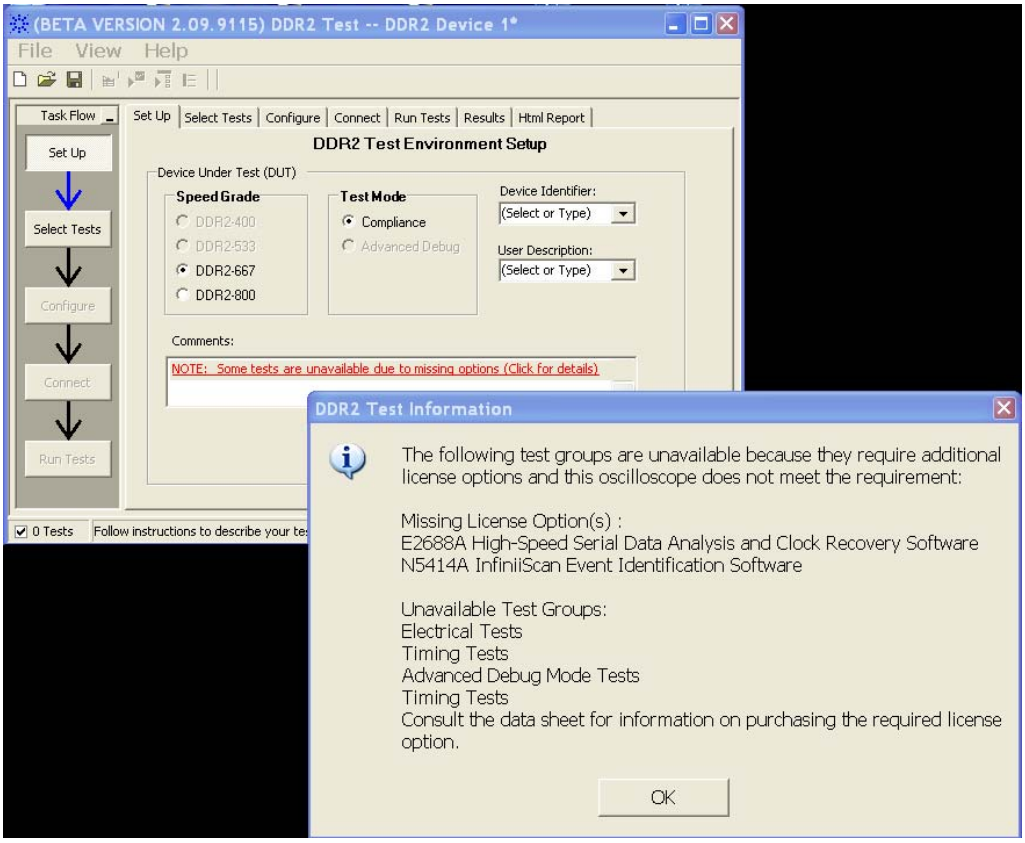

Figure 104 Software License Error

Ensure you have installed all required licenses before running the N5413A DDR2 Compliance Test Application.

Frequency Out of Range Error

You are allowed to type in the DUT data rate for the Advanced Debug Mode tests. However, if you enter an incorrect data strobe test signal frequency, the following error dialog box appears. For example, if the selected DDR2 speed grade option is DDR2-400, the expected frequency of the data strobe signal, DQS is 200MH (half of the data transfer rate). However, if the measured DQS frequency is out by +/-10% of the expected frequency value, exception will be thrown.

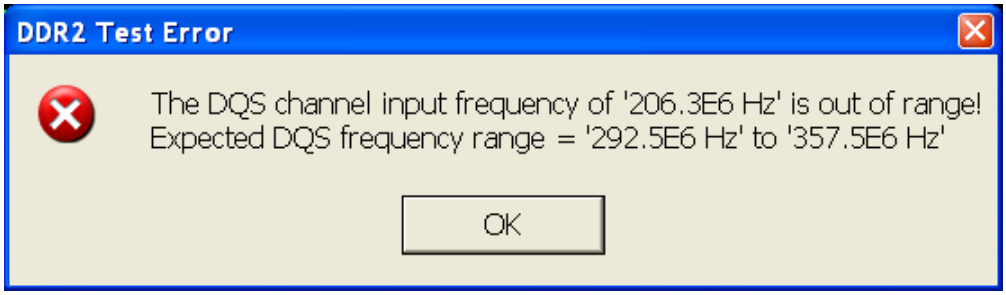

Figure 105 Frequency Out of Range Error

Type in the correct data rate, within the range, as mentioned in the error message box.

Invalid Test Mask Error

Selecting Advanced Debug as the Test Mode shows you an additional command button - **Set Mask File**. You need to select a valid test mask that can by recognized by the oscilloscope.

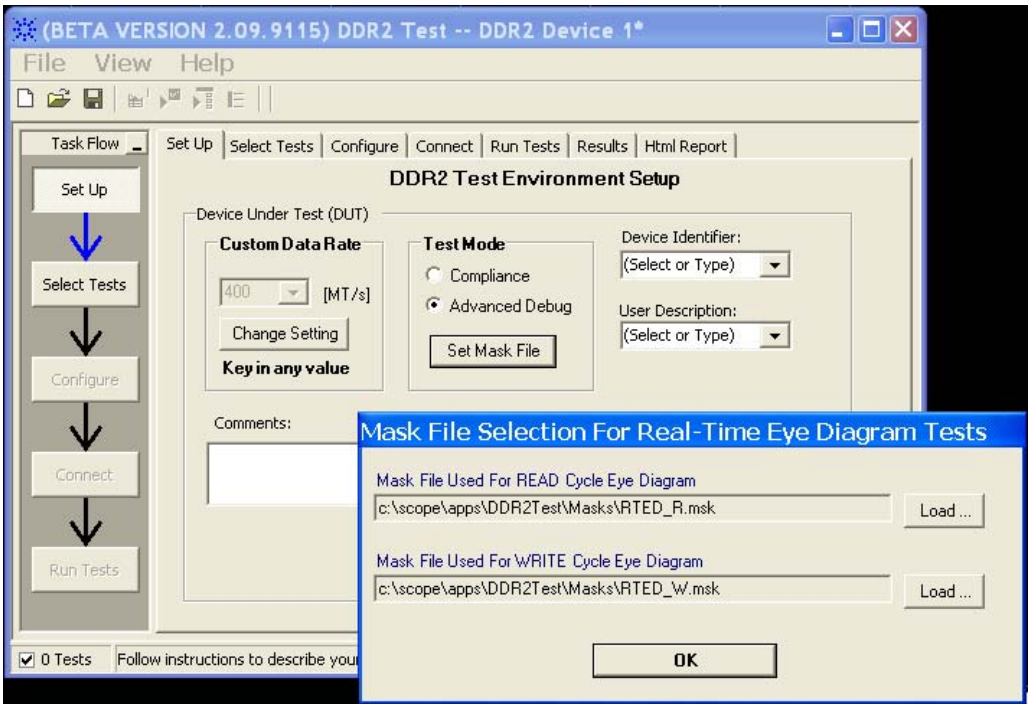

Figure 106 Selecting Mask File for Eye Diagram Tests

Attempt to load an invalid test mask will prompt you with the following error message.

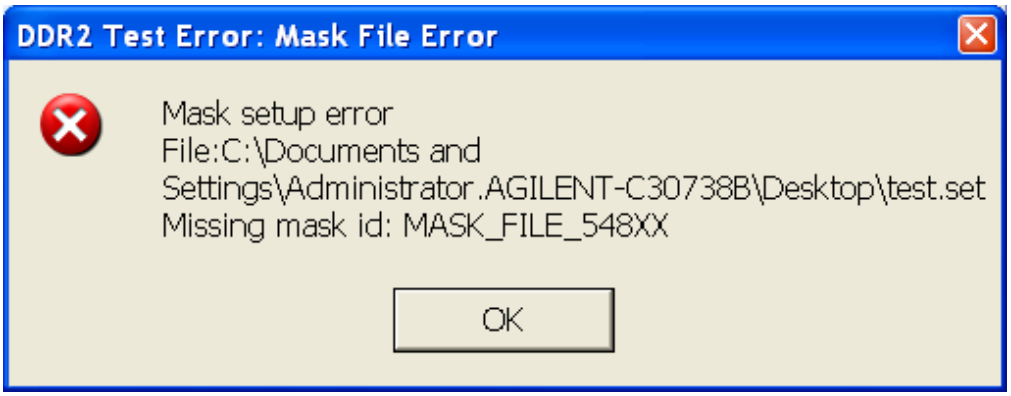

Figure 107 Selecting Mask File for Eye Diagram Tests

Missing Signal Error

This error occurs when the required signals are either not selected in the “Channel Setting” configuration or not connected to the oscilloscope. Ensure that correct channel is selected based on the signal that is physically present at the oscilloscope channel.

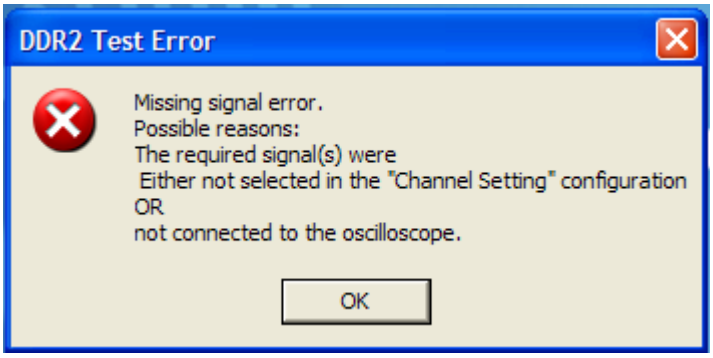

Figure 108 Missing Signal Error Message

Invalid Pre/PostAmble Signal Error

This error occurs during the multiple trial run if there is no significant voltage level transits when the driver is turned on or off during the preamble or postamble. You should verify the signals especially the DQS and DQ if they provide a valid preamble or postamble signal. If there is no significant voltage level transition when the driver is turned on or off during the pre-amble OR post-amble, the system will throw an exception to prompt user to verify the signal.

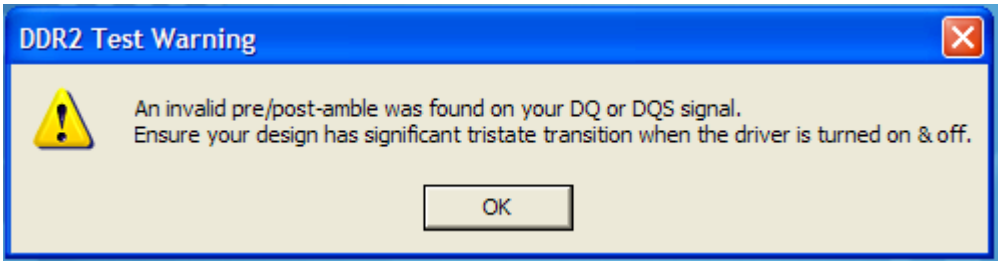

Figure 109 Invalid Pre/Post Amble Signal Error Message

You can disable this error message at the Configure tab. Turn the “Signal error message prompt” to the Disable mode. This will prevent the above error message being prompt during the multiple trial run.

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